Silicon thermo-optic phase shifters: a review of configurations and optimization strategies

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Abstract. Silicon photonics (SiPh) has emerged as the predominant platform across a wide range of integrated photonics applications, encompassing not only mainstream fields such as optical communications and microwave signal processing but also burgeoning areas such as artificial intelligence and quantum processing. A vital component in most SiPh applications is the optical phase shifter, which is essential for varying the phase of light with minimal optical loss. Historically, SiPh phase shifters have primarily utilized the thermo-optic coefficient of silicon for their operation. Thermo-optic phase shifters (TOPSs) offer significant advantages, including excellent compatibility with complementary metal–oxide–semiconductor technology and the potential for negligible optical loss, making them highly scalable. However, the inherent heating mechanism of TOPSs renders them power-hungry and slow, which is a drawback for many applications. We thoroughly examine the principal configurations and optimization strategies that have been proposed for achieving energy-efficient and fast TOPSs. Furthermore, we compare TOPSs with other electro-optic mechanisms and technologies poised to revolutionize phase shifter development on the SiPh platform.

Keywords: thermo-optic coefficient; phase shifter; silicon photonics.

1 Introduction

The use of silicon photonics (SiPh)[1–4] has witnessed exponential growth over the past decade. This increase is driven by the relentless and explosive expansion of consumer data, the necessity for real-time processing of wideband signals, and the significant energy demands of the data center industry, which consumed between 1% and 5% of global power in 2020.[5] Photonic integrated circuits (PICs) present effective solutions to these challenges, offering solutions where there is a demand for energy efficiency and high computational throughput in disruptive technologies, including optical communications transceivers,[6,7] lidar systems,[8] quantum optics devices,[9] and optical sensors.[10] In addition, emerging computing architectures for artificial intelligence and neuromorphic computing, leveraging SiPh, have shown numerous benefits—such as multiwavelength capabilities, ultrahigh speeds, and low power consumption—that address the limitations of complexity, cost, and footprint associated with traditional electronic computing components.[11]

Both mainstream and emerging applications necessitate the development of highly complex PICs that incorporate an extensive library of on-chip components such as (de)multiplexers, phase shifters, modulators, laser sources, photodetectors, and fiber-to-chip couplers. Among these, phase shifters stand out as a pivotal component in most PICs, enabling the manipulation of the real part of the effective refractive index with minimal—ideally zero—alteration to the imaginary part. The demand for components that combine ultralow optical loss with a compact footprint is critical for ensuring the scalability of advanced PICs and meeting the rigorous requirements of emerging applications. In this context, silicon thermo-optic phase shifters (TOPSs) have emerged as the prevalent method. TOPSs utilize the variation in silicon's refractive index—where light is predominantly confined—due to changes in temperature. Silicon TOPSs have become the cornerstone for the development of sophisticated PICs, showcasing the vast potential of SiPh

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technology across various application domains. Notable examples include optical reconfigurable and multipurpose photonic circuits,[9,12] phased arrays for lidar systems,[13] optical neural networks,[14] and Fourier transforming for optical spectrometry,[15] with demonstrators integrating from ~50 to 176 TOPSs.[9] However, the intrinsic heating mechanism of TOPSs often results in high power consumption and slow operation. As a consequence, various optimization configurations and strategies have been proposed to enhance power efficiency and switching speed, or both, making the topic of TOPSs a blooming area of research over the past decade.

In this review, we explore the configuration and optimization strategies that have been proposed for TOPSs in SiPh. Our discussion begins with an examination of the fundamental principles underlying thermo-optic tuning in silicon waveguides, along with basic design guidelines and the trade-offs required for achieving optimal performance. Subsequently, we delve into the advancements in various TOPS technologies, highlighting developments in metallic heaters, transparent heaters, doped silicon, folded waveguide structures, and multipass waveguide configurations. Finally, TOPSs are compared with alternative technologies, providing a comparative analysis. A concluding section is dedicated to discussing prospective technological advancements and the future outlook for TOPSs in SiPh.

2 Fundamentals

Thermo-optic phase tuning in silicon waveguides is achieved by applying localized heat and exploiting the large thermo-optic coefficient of silicon, $\sim 1.8 - 1.9 \times 10^{-4}$ K^{-1}.[16,17] It is important to note that for devices utilizing SiO$_2$ as the waveguide cladding, the thermo-optic effect of SiO$_2$ is typically disregarded since it is an order of magnitude lower than that of silicon, $\sim 9 \times 10^{-6}$.[18] The phase shift variation $\Delta\phi$ in a waveguide can be expressed as

$$\Delta\phi = \frac{2\pi}{\lambda} \Delta n_{\text{eff}} L, \tag{1}$$

where λ is the wavelength, Δn_{eff} is the variation in the effective refractive index, and L is the path length. When the phase shift is induced by a change in the waveguide temperature, it is described by

$$\Delta\phi = \frac{2\pi}{\lambda} \frac{\partial n_{\text{eff}}}{\partial T} \Delta T L, \tag{2}$$

where $\partial n_{\text{eff}}/\partial T$ is the thermo-optic coefficient of the optical mode, and ΔT represents the temperature increase.

According to joule heating, the temperature increase is directly proportional to the power consumed by the microheater, denoted as $\Delta T \propto P_{\text{elec}}$. Consequently, the power consumption of TOPSs, specifically the power required to induce a phase shift of π (P_π), can be formulated as

$$P_\pi = \frac{\lambda}{2L} \left(\frac{\partial n_{\text{eff}}}{\partial P_{\text{elec}}} \right)^{-1}, \tag{3}$$

where $\partial n_{\text{eff}}/\partial P_{\text{elec}}$ represents the variation of the effective refractive index with the electrical power applied to the microheater. For TOPSs that are invariant in the propagation direction, such variation is proportional to the active length of the heater.

Hence, in Eq. (3), the value of P_π does not significantly vary with the length of the phase shifter. This implies that the same phase shift can be achieved using either short but intensely heated active heaters or longer but mild heaters, with the electrical power required to reach the desired temperature remaining constant. However, if the phase shift architecture is designed to vary with the direction of light propagation, it is possible to disrupt this relationship and achieve higher thermo-optic efficiencies while maintaining the same active footprint.

To assess the performance of TOPSs, the following figure of merit (FOM) is commonly employed and aimed to be minimized:

$$\text{FOM} = P_\pi \tau, \tag{4}$$

where P_π represents the power required to induce a phase shift of π, typically expressed in milliwatts (mW), and τ denotes the switching time, measured in microseconds (μs). On the other hand, to experimentally determine the performance metrics of the phase shifters, these devices are often integrated into interferometric structures, such as Mach–Zehnder interferometers (MZIs), microring resonators (MRRs), or multimode interferometers (MMIs).

3 Basic Configurations

The fundamental design of a TOPS typically involves a straight silicon waveguide accompanied by a parallel heater, resulting in a device that is invariant along the propagation direction. The heater is constructed from an electrically conductive material, designed to allow the flow of an electrical current and consequently generate joule heating, described by the equation $P_h = I_h^2 R_h$, where I_h represents the current flowing through the heater, and R_h denotes the resistance of the heater. In addition, an alternative approach to heater design involves doping the silicon waveguide itself, thereby enabling the waveguide to function as the heater by facilitating electrical conductivity and heat generation directly within the silicon.

In the context of a propagation-invariant configuration for TOPSs, the power consumption can be analytically approximated, as detailed by Jacques et al.,[19] by the equation,

$$P_\pi \approx \Delta T_\pi G A, \tag{5}$$

where G represents the thermal conductance between the heated waveguide and the surrounding materials, and A denotes the area through which the heat flow occurs. Similarly, an analytical expression for the switching speed, τ, can be derived, indicating its dependence on the thermal properties and geometry of the system,[19]

$$\tau \approx \frac{H}{G} \propto \frac{AL}{G}, \tag{6}$$

in which H, the heat capacity of the heated waveguide, is proportional to the product of the area, A, and the length, L, of the waveguide ($H \propto AL$).

To minimize power consumption in TOPSs, it is crucial to incorporate waveguides with materials of low thermal conductivity and to minimize the distance between the waveguide and the heater. However, reducing the distance between the heater and the waveguide often results in a trade-off, as it may increase optical loss due to heater absorption. Conversely,

using materials with low thermal conductivity can indeed reduce power consumption but at the cost of slower switching speed. Therefore, unless the gap between the heater and the waveguide is diminished, a distinct trade-off between power consumption and switching speed exists. According to Eqs. (5) and (6), one potential strategy to achieve faster switching speeds without escalating power consumption involves decreasing the heat capacity of the waveguide, which suggests the use of shorter active lengths. However, this approach entails challenges. By analyzing Eq. (2), it is evident that $L_\pi \propto 1/\Delta T_\pi$. In this regard, opting for short heater lengths can give rise to critical temperature values. High temperatures can compromise the performance of the heater caused by the self-heating phenomenon produced by the increase of the heater resistance with the temperature.[18] Therefore, the actual temperature increase is lower than expected, assuming a constant heater resistance and thereby yielding a different phase shift. In addition, employing such compact phase shifters increases the susceptibility of adjacent structures to thermal cross talk, potentially affecting the overall device performance.

Several optimization strategies to enhance power consumption, switching speed, or both, have been explored in the literature, as we discuss in the Secs. 3.1–3.3. Initially, we examine the use of metallic heaters to decrease power consumption by reducing the thermal conductance of the surrounding waveguide environment. This approach, however, results in a longer switching speed. Subsequently, we explore the application of transparent heaters, which aim to diminish the gap between the heater and the waveguide, i.e., the area A traversed by

the heat flow [refer to Eqs. (5) and (6)], without penalizing the optical loss of the device. The final approach involves direct heating of the silicon waveguide through doping, thereby transforming it into a resistive element. This technique offers significant improvements in both power consumption and switching speed by minimizing the value of A, though it introduces optical loss due to free carriers. It is important to note that this direct heating approach is specific to the SiPh platform and is not applicable to other emerging photonics platforms, such as silicon nitride. Unless specified otherwise, the results discussed herein pertain to transverse electric (TE) polarization at a wavelength of ∼1550 nm.

3.1 Metallic Heaters

The most commonly employed method for inducing localized heating in a silicon waveguide or structure involves the use of metallic heaters and the principle of joule heating [Fig. 1(a)]. Such resistive heaters are typically configured as metal wires placed atop the silicon structure, separated by an intermediate dielectric layer, such as SiO_2, to mitigate optical loss [Fig. 1(b)]. The thickness of these heaters is generally on the order of ∼100 nm, determined by standard fabrication techniques, including lift-off procedures. In addition, a diverse range of metals or metallic compounds compatible with complementary metal–oxide–semiconductor (CMOS) fabrication technology can be utilized for the heaters. These materials include copper (Cu), nickel silicide (NiSi), platinum (Pt), titanium (Ti), titanium nitride (TiN), and tungsten (W). Figure 1(c) shows the temperature
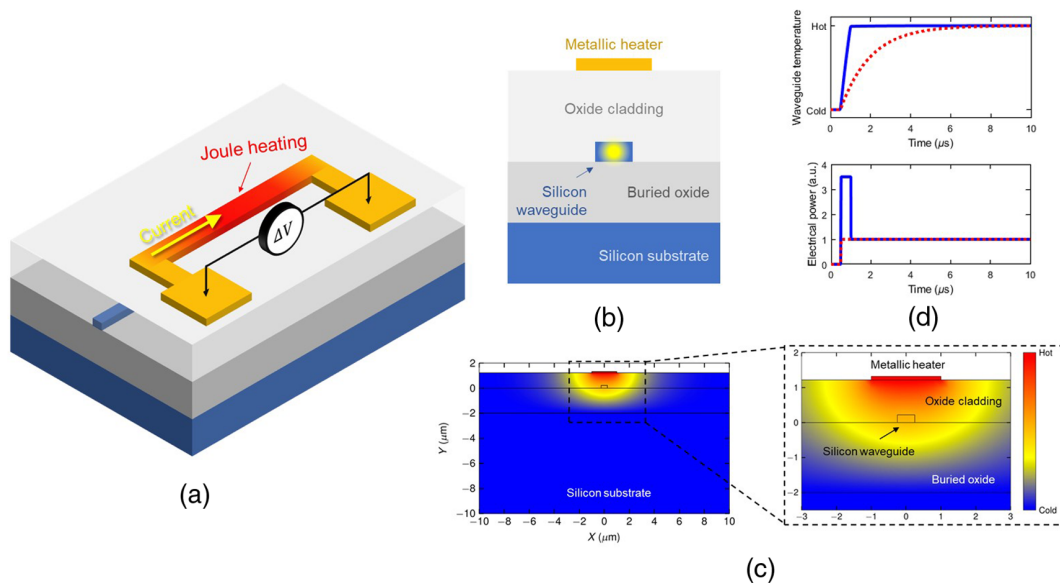

Fig. 1 (a) Illustration of a TOPS using a metallic heater on top of the waveguide. (b) Cross section of the TOPS. (c) Simulated temperature distribution of the TOPS. (d) Temporal response of the TOPS upon a square electrical signal applied to the heater with (solid blue line) and without (dotted red line) employing pulse pre-emphasis. The considered TOPS comprises a 500 nm × 220 nm Si waveguide with a 2 μm × 100 nm Ti heater on top. The gap between the waveguide and the heater is 1 μm. The temperature distribution in the cross section was obtained by solving the conductive heat equation using the COMSOL Multiphysics simulation tool. We considered the thermal constants reported in the literature.[20] A nonuniform tetrahedral mesh, with element sizes ranging from 1 to 500 nm, was employed. A conductive heat flux boundary condition with a heat transfer coefficient of 5 W/(m² K) was set on the surface. The temperature of the remaining boundaries was fixed at 293.15 K (cold).

distribution within a typical TOPS based on a metallic heater, featuring a 1-μm-thick oxide cladding layer situated between the silicon waveguide and the metallic heater.

Table 1 surveys the experimental works that have employed metallic heaters alongside various generic optimization strategies to develop phase shifters in straight silicon waveguides. It is important to note that while the focus of these studies is on the use of metallic heaters, the optimization strategies outlined are versatile and can be applied to other methodologies discussed in subsequent sections.

Espinola et al.[21] provided one of the pioneering experimental demonstrations of TOPSs on silicon nearly two decades ago. The design featured a silicon waveguide with a Cr/Au heater measuring 14 μm in width and 100 nm in thickness, positioned atop the waveguide. The phase shifter spanned a length of 700 μm, separated from the heater by a 1-μm-thick layer of SiO_2. Integrated within an MZI to function as a switch, the device exhibited significant optical loss (32 dB), which the authors attributed primarily to scattering caused by considerable sidewall roughness in the waveguide. Despite its status as one of the initial experimental reports in this field, the device demonstrated a power consumption of 50 mW and a switching time of 3.5 μs, resulting in a FOM of 175 mW μs. Notably, subsequent studies have reported similar, or at times, inferior performance metrics.[22,23]

On the application side, the capabilities of TOPSs have been harnessed for switching purposes by cascading 1×2 MZI switches to implement $1 \times N$ configurations.[23] A significant advantage of these switches lies in their compact design, with the phase shifter elements measuring only 40 μm in length. Nonetheless, these devices were characterized by considerable

power consumption and slow switching speeds, reported at 90 mW and 100 μs, respectively. The primary factor contributing to such a suboptimal performance is the substantial width of the heaters, $\sim$20 μm, which enlarges the cross-sectional area A of the phase shifter, as shown in Eqs. (5) and (6). A notable improvement in power consumption and switching speed—to 40 mW and 30 μs, respectively—can be achieved by reducing the heater width to 5 μm, as demonstrated in subsequent studies.[25]

Atabaki et al.[26] have highlighted the substantial influence of the heater width and the intermediate layer on the performance of TOPSs equipped with metallic heaters atop silicon waveguides. Narrow heaters, with widths of less than $\sim$2 μm, are shown to enable faster switching time ($\sim$4 μs) and lower power consumption ($\sim$16 mW), attributed to the reduced volume of heating. However, reducing the heater width below 2 μm does not yield significant further improvements, primarily due to the lateral heat diffusion, which spans $\sim$1 to 2 μm, thus becoming comparable to the microheater's dimensions.

Furthermore, the selection of material for the waveguide cladding plays a critical role in modulating both power consumption and switching speed, establishing a trade-off with the thermal conductivity of the cladding material. Enhancing the thermal conductivity, while keeping the specific heat capacity constant, accelerates the phase shifter's response but increases power requirements [refer to Eqs. (5) and (6)]. Substituting SiO_2 with SiN is one strategy to enhance switching speed. Moreover, applying high-energy-pulsed drive signals can further decrease switching time, potentially to submicrosecond scales, as demonstrated by the use of a pre-emphasis pulse [illustrated in Fig. 1(d)]. This approach swiftly achieves the steady-state operation, although the inherent delay in heat transfer from the

Table 1 Summary of basic experimental TOPSs using metallic heaters in SiPh.

Ref.	Structure/heater metal	Optimization strategy	Loss (dB)	P_π (mW)	Switching time (μs)[a]	FOM (mW μs)	Length (μm)
21	MZI/CrAu	None	32[b]	50	3.5	175	700
22	MZI/N/A	None	12[b]	235	60	14×10^3	2500
23	MZI/N/A	None	22[b]	90	100	9000	140
24	MRR/Ti	Air trenches	N/A	$\sim$10	$\sim$10	$\sim$100	$\sim$30
25	MZI/Pt	None	16[b]	40	30	1200	40
26	MRR/Ni	Pulse pre-emphasis	<1	16	4[c] /<1[d]	64[c] /<16[d]	$\sim$60
27	MZI/Pt	Free-standing	2.8[b]	0.54	141	76	100
28	MRR/Ti	Free-standing	<1	1.2	170	204	50
29	MZI/NiSi	Close heater	<1	20	3	60	200
30	MZI/TiN	Free-standing	<1	0.49	144	71	1000
31	MRR/NiSi	Free-standing	<1	2.9	358	1038	50
32	Microdisk NiCr	Close heater and pulse pre-emphasis	<1	12	2.9[c]/0.085[d]	35[c]/1[d]	$\sim$60
33	MZI/W	None	<1	22	45	990	200
19	MZI/TiN	Geometry	<1	30	7	210	320

N/A, not available; MZI, Mach–Zehnder interferometer; MRR, microring resonator.

[a]We consider the limiting switching speed of the switch in the case that the value of the phase shifter is not reported, i.e., the highest value between the rise and fall time constants.

[b]The value corresponds to the entire switching device. The optical loss of the phase shifter is not reported.

[c]Without pre-emphasis.

[d]With pre-emphasis.

heater to the silicon waveguide sets a lower bound on achievable switching time.

The employment of parallel heaters alongside the silicon waveguide has been showcased as a method to realize low-loss, energy-efficient, and fast phase shifters.[29] This approach utilizes a rib waveguide configuration instead of the conventional strip design, with heaters positioned on both sides of the waveguide's thin bottom slab. In Ref. [28], the heaters were composed of a 20-nm-thick NiSi layer, featuring widths varying from 500 nm to 3 μm. Notably, a layer of SiN is deposited atop the silicon waveguide prior to heater formation to inhibit silicide development within the waveguide structure. By setting the distance between the heaters and the waveguide at 500 nm, a balance between low optical loss and a remarkable FOM of 60 mW μs was attained, accompanied by a power consumption of 20 mW and a switching time of 3 μs. Despite the phase shifter's relatively high propagation loss of 25 dB/cm, its compact length (40 μm) resulted in an insertion loss of less than 1 dB.

Lower FOM values have also been reported through the strategic placement of metallic heaters directly atop the silicon structure, leveraging silicon's thermal conductivity,[32] achieving a power consumption of merely 12 mW and a switching time of 2.9 μs. To circumvent optical losses associated with NiCr heaters, a microdisk with a 4 μm diameter was utilized as the phase-shifting element, minimizing metal–light interactions to less than 1 dB of loss due to the evanescent nature of the optical mode toward the device's center.

The application of the pre-emphasis technique, as previously mentioned,[26] further reduces the switching time to 85 ns (FOM $\approx$ 1 mW μs), enhancing the responsiveness of ON/OFF switching devices based on thermal phase shifters. Such devices benefit from differential or balanced architectures, enabling optical changes by selectively heating one of the optical paths. However, the primary challenge lies in the cooling period required for the heaters, as simultaneous cooling of both paths is essential before initiating the next switch to prevent continuous device heating.

The selection of an appropriate metal for the heaters is crucial not only from the perspective of minimizing optical loss but also to ensure that electrical power dissipation occurs predominantly within the heater rather than in the interconnections. While the optical loss may not be significantly affected by the choice of heater metal, the efficiency of power dissipation is paramount. The integration of the heater metal into a CMOS process flow is a critical consideration when selecting the optimal material for the heater. Although tin- and nickel-based alloys can be patterned as heaters within a CMOS process, foundries often prefer Cu and W due to their more desirable characteristics.

W, in particular, is favored for its relatively high resistivity and melting point, offering enhanced stability for the heaters.[33] This stability is beneficial for devices that require consistent performance over time. In addition, W heaters can be electrically interconnected with Cu wires, taking advantage of Cu's lower resistivity to ensure that most of the heat is dissipated in the W heater. This configuration maximizes the thermal efficiency of the device.

Masood et al.[33] demonstrated the effectiveness of W heaters in a silicon waveguide, fabricated using a CMOS-like layer stack without further optimization. The devices exhibited power consumption levels of around 22 mW and switching time of ~40 μs. The optical loss was reported to be less than 1 dB, with excellent electrical stability observed over 750 switching cycles.

Thermal cross talk is a critical consideration in densely packed PICs, where the proximity of devices can lead to undesirable interference due to heat diffusion. Depending on the TOPS configuration, the minimum thermal cross talk between devices can range between less than 10 to 50 μm.[19,34] Although utilizing longer heaters can decrease the temperature difference required to achieve a phase shift of π as indicated by Eq. (2), this approach also expands the device's footprint and potentially increases optical loss. Thus, achieving an optimal balance among device specifications necessitates careful consideration and judicious optimization.

A strategy to mitigate parasitic thermal phase shifts involves the implementation of deep trenches between the aggressor (source of thermal interference) and victim (affected device) components.[19] This technique effectively isolates devices thermally, minimizing cross talk without compromising the compactness or performance of the circuit. By employing such structural modifications, PIC designers can enhance device integration density while maintaining control over thermal effects, ensuring that each component functions as intended with minimal interference.

The thermal isolation of phase shifters, achieved through the implementation of air trenches or by detaching the structure from the substrate via an undercut [illustrated in Figs. 2(a) and 2(b)], significantly decreases power consumption. This reduction is due to the air's thermal conductivity being nearly 2 orders of magnitude lower than that of SiO$_2$ ($\sim$0.025 Wm^{-1} K^{-1}), thereby concentrating and elevating the temperature within the silicon waveguide, as depicted in Fig. 2(c). However, it is important to note that this approach leads to an increase in switching time [as indicated by Eqs. (5) and (6)]. Despite this drawback, such thermal optimization strategies are particularly beneficial for deploying multiple phase shifters within applications where moderate total power consumption is prioritized over rapid switching speeds.

A straightforward method for achieving thermal isolation involves deep etching on both sides of the waveguide, preserving the conventional heater-waveguide layout. Following this approach, devices have demonstrated power consumption and switching speeds around 10 mW and 10 μs, respectively.[24] Moreover, submilliwatt power consumption (0.54 mW) has been reported for waveguides released from the substrate.[27] These freestanding phase shifters, supported by two SiO$_2$ struts across a 320-μm-long released waveguide, exhibit mechanical stability. However, this configuration results in the extended switching time, increasing from 39 μs in the attached version to 141 μs upon release. Recent studies have reported similar outcomes for released switching structures,[28,30,31] underscoring the trade-offs between power efficiency, switching speed, and structural design in the development of TOPSs.

3.2 Transparent Heaters

Transparent heaters, i.e., electrically conductive materials with minimal optical loss in the near-infrared region, provide a strategic avenue to mitigate the trade-off between optical loss, power consumption, and switching speed in TOPSs. This approach facilitates placing the heater in close proximity to the silicon waveguide, as illustrated in Figs. 3(a) and 3(b), significantly reducing both the temperature gradient and the diffusion
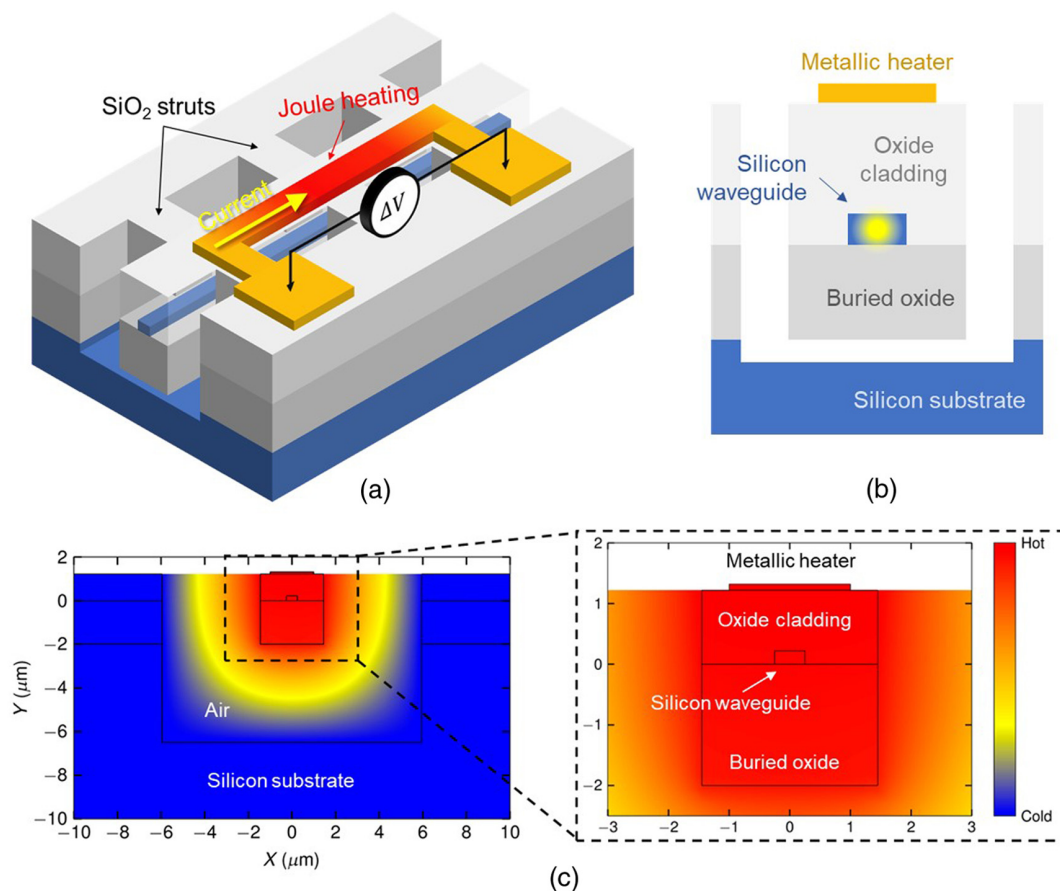
Fig. 2 (a) Illustration of a TOPS using a metallic heater on top of the waveguide with thermal isolation by etching the top cladding and buried oxide. (b) Cross section of the free-standing TOPS. (c) Simulated temperature distribution of the free-standing TOPS. The considered TOPS comprises a 500 nm × 220 nm silicon waveguide with a 2 μm × 100 nm Ti heater on top. The gap between the waveguide and the heater is 1 μm. The temperature distribution in the cross section was obtained by solving the conductive heat equation using the COMSOL Multiphysics simulation tool. We considered the thermal constants reported in the literature.[20] A nonuniform tetrahedral mesh, with element sizes ranging from 1 to 500 nm, was employed. A conductive heat flux boundary condition with a heat transfer coefficient of 5 W/(m^2 K) was set on the boundaries in contact with air. The temperature of the remaining boundaries was fixed at 293.15 K (cold).

time between the waveguide and the heater. Consequently, this configuration not only improves the efficiency of heat transfer but also enhances the switching time of the phase shifter by shortening the thermal diffusion pathway.

Transparent heaters can be constructed using either two-dimensional (2D) materials or transparent conducting oxides (TCOs). 2D materials, such as graphene and carbon nanotubes (CNTs), offer the advantage of low optical loss due to their exceptional optical properties and atomic-scale thickness while also being electrically conductive. However, fabricating heaters from graphene presents challenges not encountered with traditional metal heaters. Typically, graphene heaters are produced by synthesizing a monolayer through chemical vapor deposition and subsequently transferring it onto the photonic chip, followed by precise patterning. It is important to note that the optical and electrical characteristics of graphene heaters are significantly influenced by the quality of the graphene sheet.

By contrast, TCOs such as indium tin oxide (ITO) are widely utilized in various optoelectronic applications, including photovoltaic cells and displays, due to their well-established and mature fabrication techniques, such as sputtering. TCOs combine transparency in the visible to near-infrared range with good electrical conductivity, making them suitable for integration into photonic devices.

Table 2 summarizes the main specifications for experimental TOPSs in silicon that utilize transparent materials for heating.

Graphene, renowned for its electrical conductivity, also boasts a remarkable thermal conductivity of ~5000 Wm^{-1} K^{-1}.[42] Initial propositions for incorporating graphene into silicon waveguides for thermo-optic tuning aimed to exploit its thermal conductance, envisioning a graphene layer to bridge the metallic heater and the silicon waveguide for more effective heat transfer.[35] Despite these efforts, experimental outcomes indicated power consumption exceeding 50 mW and a moderate switching speed of 20 μs, failing to surpass the performance
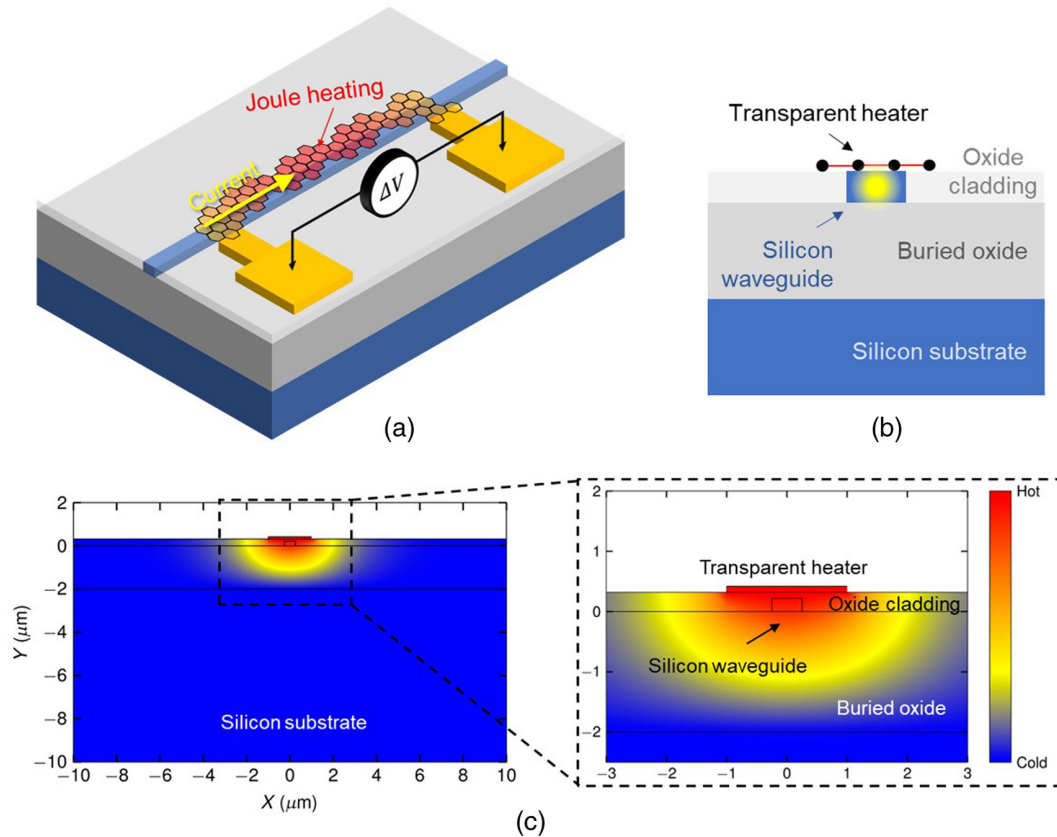
Fig. 3 (a) Illustration of a TOPS using a transparent heater directly on top of the waveguide. (b) Cross section of the TOPS. (c) Simulated temperature distribution of the TOPS using an ITO heater. The considered TOPS comprises a 500 nm × 220 nm silicon waveguide with a 2 μm × 100 nm ITO heater on top. The gap between the waveguide and the heater is 100 nm. The temperature distribution in the cross section was obtained by solving the conductive heat equation using the COMSOL Multiphysics simulation tool. We considered the thermal constants reported in the literature.[20] A nonuniform tetrahedral mesh, with element sizes ranging from 1 to 500 nm, was employed. A conductive heat flux boundary condition with a heat transfer coefficient of 5 W/(m² K) was set on the surface. The temperature of the remaining boundaries was fixed at 293.15 K (cold).

Table 2 Summary of basic experimental TOPSs using transparent heaters in SiPh.

Ref.	Structure/heater material	Gap (nm)	Loss (dB)	P_π (mW)	Switching time (μm)[a]	FOM (mW μs)	Length (μm)
35	MZI/metal + graphene	0	5[b]	>50	20	>1000	120
35	Microdisk/graphene	0	<1	23.5	13	305.5	~5
36	MRR/graphene	240	<1	11	3.5	38.5	~55
37	MZI-PhCW/graphene	11	1.1	2	<1	<2	20
38	PhCC/graphene	0	2	N/A	1.5	N/A	5
39	MRR/CNTs	0	N/A	14.5	4.5	65.3	~315
40	MRR/MoS$_2$	30	~0.42	7.5	25	187.5	~283
20	MZI/ITO	660	~0.01	9.7	5.2	50.44	50
41	MZI/IHO	0	~0.5	9.6	0.98	9.41	10

N/A, not available; MZI, Mach–Zehnder interferometer; MRR, microring resonator; PhCW, photonic crystal waveguide; PhCC, photonic crystal cavity; CNTs, carbon nanotubes; MoS$_2$, molybdenum disulfide; ITO, indium tin oxide; IHO, hydrogen-doped indium oxide.

[a]We consider the limiting switching speed of the switch in the case that the value of the phase shifter is not reported, i.e., the highest value between the rise and fall time constants.

[b]Value obtained through numerical simulation.

of conventional metal-based phase shifters. In addition, numerical simulations revealed that the graphene layer could induce optical losses around 5 dB, further challenging its practicality for this application.

Subsequent advancements were made by adopting a similar approach and silicon structure as outlined in Ref. 31, where a graphene heater was implemented atop a silicon microdisk, replacing the metallic counterpart.[43] This configuration achieved a power consumption of 23.5 mW and a switching speed of $\sim$10 μs, with the insertion loss attributable to the graphene heater being negligible ($<2 \times 10^{-4}$ dB/μm). This minimal interaction between the heater and the optical mode of the microdisk resonator contributed to the device's enhanced performance.

A breakthrough was reported with the use of a graphene heater on a silicon waveguide, achieving a record FOM value of less than 40 mW μs ($P_\pi = 11$ mW and $\tau = 3.5$ μs).[36] The design included two intermediate layers, HSQ and Al_2O_3, positioned between the silicon waveguide and the graphene heater, with a meticulously optimized gap of 240 nm to maximize performance while minimizing optical loss. It is noteworthy that the reported power consumption was characterized at a wavelength of $\lambda = 1310$ nm, with potential variations at $\lambda = 1550$ nm due to differences in optical mode confinement.

Beyond graphene, CNTs have been proposed as an alternative for crafting transparent heaters, offering the principal advantage of lower absorption in the near-infrared spectrum. Direct integration of CNTs atop silicon waveguides has been explored for thermo-optic tuning purposes.[39] Despite their promising optical properties, a significant limitation of CNTs is their incompatibility with standard CMOS fabrication processes. Moreover, the performance metrics reported, including a power consumption of 14.5 mW and a switching speed of 4.5 μs, do not exhibit marked improvements over analogous devices based on graphene.

Transition-metal dichalcogenides, particularly a single layer of MoS_2 (molybdenum disulfide), have shown better prospects as heater materials when positioned in close proximity (30 nm) to the silicon waveguide.[40] This configuration yielded an impressively low power consumption of 7.5 mW in a 283-μm-long MoS_2 microheater, alongside a minimal insertion loss of $\sim$0.42 dB. However, the relatively slow response time of the phase shifter, around 25 μs, can be attributed to the Schottky contact formed between the MoS_2 layer and the Au electrical pads. Future enhancements could potentially be realized by establishing ohmic contacts with low resistance, optimizing the device's performance further.

The synergy between transparent heaters and the augmentation of light–matter interactions through slow-light phenomena offers a pathway to substantial improvements in the power efficiency and speed of TOPSs. The slow-light effect, facilitated by the elevated group index in photonic crystal waveguides (PhCWs), enhances tuning efficiency dramatically. As a result, switching time under 1 ms and power consumption as low as 2 mW (yielding a FOM of less than 2 mW μs) have been achieved in ultracompact phase shifters, measuring merely 20 μm in length, based on a PhCW integrated with a graphene heater.[37] The minimal gap of only 11 nm between the heater and the PhCW contributes to this high efficiency, despite the graphene layer, inducing an optical loss of 1.1 dB.

Furthermore, ultracompact device switches can be realized through the development of a photonic crystal cavity (PhCC).[38] This innovative approach allows for a switching power, defined as the energy required to transition from a low loss state to a high loss state, to be less than 2 mW, coupled with a switching speed of $\sim$1.5 μs for a device with a footprint of only 5 μm.

TCO-based microheaters stand out for their CMOS-compatible manufacturing processes and thermo-optical characteristics. A key advantage of TCOs, such as ITO, resides in their capacity to modulate the concentration of mobile electrons within the near-infrared spectrum. This unique property enables these materials to function akin to metals with minimal loss at the operational wavelengths of devices, thus mitigating the optical losses typically associated with metal-based heaters. As a result, the spacer between the silicon waveguide and the heater can be substantially reduced, enhancing power efficiency and switching speed without incurring the significant optical losses characteristic of thinner metal gaps.[20] Specifically, a compact ITO/Si TOPS, measuring only 50 μm in length, demonstrated a power consumption of 9.7 mW and a switching time of 5.2 μs.

Further advancements were achieved with the introduction of a hydrogen-doped indium oxide (IHO) microheater, implemented directly atop the waveguide.[41] This 10-μm-long IHO heater not only showcased an insertion loss of $\sim$0.5 dB but also achieved a submicrosecond switching speed (0.98 μs) while consuming 9.6 mW. Consequently, this led to an exceptionally low FOM of 9.41 mW μs.

3.3 Doped Silicon

Doped silicon serves a dual purpose in the topic of TOPSs, acting simultaneously as both the heater resistor and the silicon waveguide. The doping process, which can involve n-type or p-type dopants such as arsenic (As), boron (B), or phosphorus (P), introduces free carriers into the silicon, leading to inherent optical losses. This effect creates a fundamental trade-off between the resistivity of the heaters and the optical absorption they introduce. To achieve a balance that minimizes optical losses while ensuring resistance values are compatible with electrical drivers and intended applications, silicon is typically doped to a carrier concentration of $\sim$10^{18} cm^{-3}. In addition, employing multiple heater resistors in parallel is a common strategy to lower the total resistance, enhancing the device's compatibility with electrical systems [illustrated in Fig. 4(a)].

It is important to note that doped silicon heaters exhibit specificity toward the silicon photonic platform and may not be directly transferable to other photonic materials such as silicon nitride. Table 3 compiles experimental studies that have utilized doped silicon as the heating element, detailing their main specifications.

Employing doped silicon wires as heaters presents a viable alternative to traditional metallic heaters. Such resistive elements are typically built by doping the edges of a rib waveguide, maintaining a distance of less than 1 μm from the core to mitigate excessive optical loss, while the central region of the waveguide remains undoped. Consequently, the electrical current flows parallel to the waveguide's length. This configuration allows for power consumption levels comparable to those of metallic heaters positioned atop the waveguide ($\sim$20 mW) but offers the advantage of faster switching speeds (ranging from 2 to 5 μs). The enhanced speed is attributable to the reduced distance over which heat must propagate.[19,47]

On the other hand, doped silicon waveguides can facilitate even faster switching through direct current injection. This approach enables heat generation directly within the waveguide
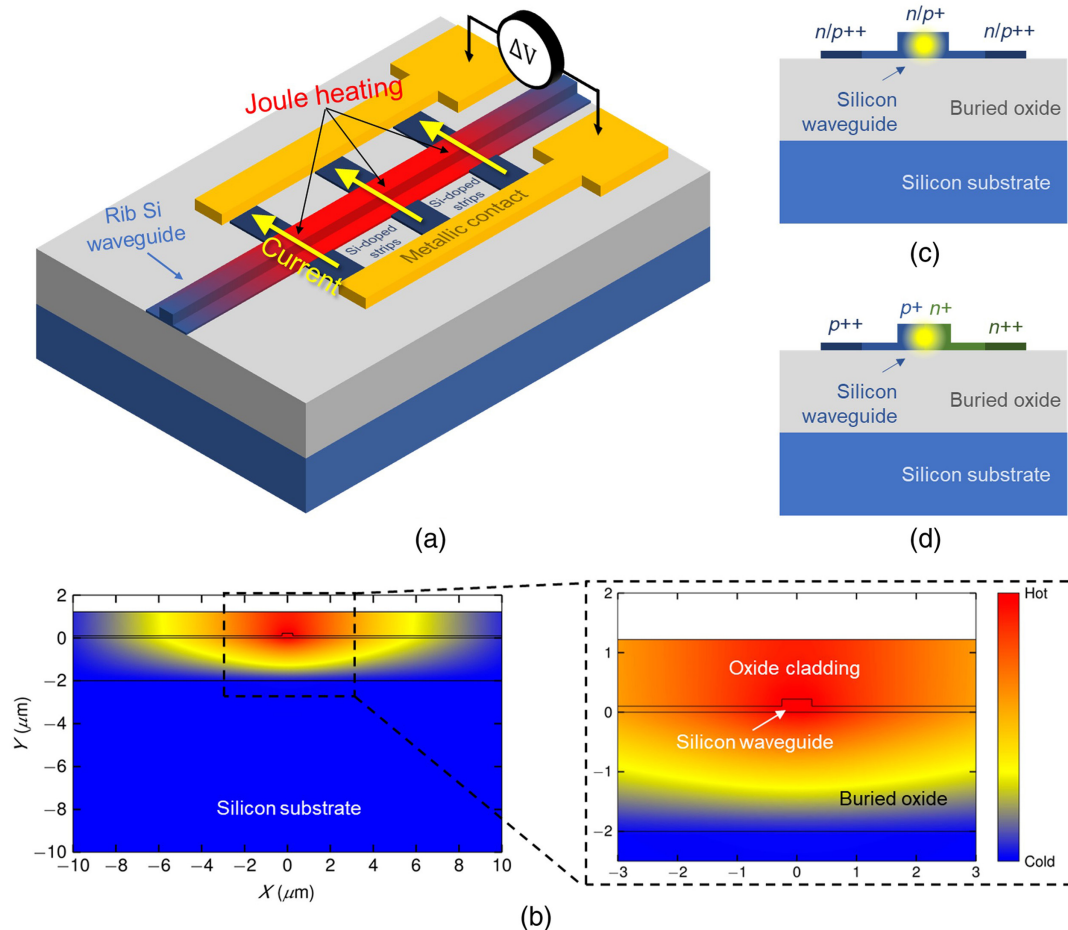
Fig. 4 (a) Illustration of a TOPS utilizing a silicon-doped heater, where the heat generation occurs within the doped silicon waveguide. In this configuration, the waveguide is of the rib type, with several silicon-doped heaters arranged in electrical parallel to minimize total resistance. Metallic contacts are linked to the silicon waveguide via silicon-doped strips. (b) Simulated temperature distribution within the TOPS, consisting of a 500 nm × 220 nm silicon waveguide atop a 100-nm-thick slab, with 1 μm-thick SiO$_2$ cladding. Temperature distribution analysis was performed by solving the conductive heat equation with the COMSOL Multiphysics simulation tool, considering the waveguide core as the heat source, based on thermal constants from the literature.[20] A nonuniform tetrahedral mesh, with element sizes ranging from 1 to 500 nm, was employed. A conductive heat flux boundary condition, with a heat transfer coefficient of 5 W/(m^2 K), was applied on the surface, while the temperature for all other boundaries was fixed at 293.15 K (cold). (c), (d) Cross-sectional views of the TOPS featuring (c) direct current injection and (d) a pn junction setup.

itself, as depicted in Fig. 4(b), effectively bypassing the limitations associated with heat propagation from external sources. In addition, this approach offers a slight reduction in power consumption compared with parallel heaters adjacent to the silicon waveguide. Rib waveguides, characterized by heavily doped edges and a lightly doped center, are essential for facilitating electrical current injection into the waveguide, as depicted in Fig. 4(c). This doping configuration ensures an optimal overlap between the thermal profile and the optical mode, minimizing the optical loss due to free carriers.

The phase shifter may also be designed as a series of individual resistors in parallel, allowing for customization of the device's resistance and driving voltage/current by adjusting the number of unit cells independently of its length. Such configurations have achieved insertion losses as low as 0.2 dB, power

consumption of around 25 mW, and switching time of ~3 μs.[46] Optimizing the waveguide geometry further reduces power consumption without significantly affecting optical loss or switching speed. Notably, power consumption was minimized to 12.7 mW using a compact silicon-doped heater, ~10 μm in length, integrated directly into the waveguide. An adiabatic bend was employed to minimize optical loss from free-carrier absorption and avoid optical mismatch, thereby preventing undesired reflections or the excitation of higher-order modes.[45]

Moreover, leveraging the field pattern distribution in MMI devices facilitates achieving low insertion loss, compact footprints, and fast switching. Electrical connections are strategically placed at positions corresponding to field pattern minima within the MMI. A 35-μm-long device demonstrated power consumption and switching time of 29 mW and 2 μs, respectively,

Table 3 Summary of basic experimental TOPSs using doped silicon heaters in SiPh.

Ref.	Structure	Dopant/concentration	Current injection	Loss (dB)	P_π (mW)	Switching time (μm)[a]	FOM (mW μs)	Length (μm)
44	MZI	p-type (B)/10^{18} cm^{-3}	Direct	3	6	0.6	3.6	115
45	MRR	n-type (As)/1.8×10^{18} cm^{-3}	Direct	0.5	12.7	2.4	30.5	~10
46	MZI	p-type (B)/7×10^{17} cm^{-3}	Direct	~0.2	~25	~3	~75	61.6
47	MZI	n-type (N/A)/N/A	Parallel heaters	N/A	25	5	125	100
48	MRR	p- and n-type (N/A)/2×10^{18} and 4×10^{17} cm^{-3}	Direct with pn junction	N/A	19.5	0.45	7.8	~125
49	MRR	n-type (As)/4×10^{13} cm^{-2}	Direct with pn junction	2.5	14	4	56	3.4
50	MZI	p- and n-type (N/A)/N/A	Parallel heater with pn junction	1.6[b]	20.9	97.5	~2000	50
19	MZI	n-type (P)/10^{20} cm^{-3}	Parallel heaters	<0.4	22.8	2.2	50.2	320
51	MZI	p-type (P)/10^{18} cm^{-3}	Direct	2	29	2	58	35
52	MZI	p-type (N/A)/10^{18} cm^{-3}	Direct	0.24	22.6	0.5	11.3	~15

N/A, not available; MZI, Mach–Zehnder interferometer; MRR, microring resonator.
[a]We consider the limiting switching speed of the switch in the case that the value of the phase shifter is not reported, i.e., the highest value between the rise and fall time constants.
[b]The value corresponds to the entire switching device. The optical loss of the phase shifter is not reported.

with a moderate insertion loss of 2 dB.[51] Subsequent improvements reduced the insertion loss to below 1 dB by minimizing the number of electrical connections, while the switching speed was enhanced to 500 ns through the incorporation of a thin Al heat sink.[52]

Integrating a pn junction within a silicon waveguide, as illustrated in Fig. 4(d), enhances the operational stability of TOPSs. The saturated I–V response characteristic of pn junctions serves as a safeguard against thermal runaways by inherently limiting the current flow. Furthermore, the diode-like behavior of the junction facilitates the independent driving of multiple heaters using the same electrical pads.[50] This configuration involves two diode heaters arranged in parallel, with the cathode of one heater connected to the anode of the other and vice versa, allowing for selective heating by simply reversing the voltage polarity. Reported configurations demonstrated power consumption of ~21 mW and switching speeds nearing 100 μs.[50] To decrease the overall resistance and, consequently, the required driving voltage, a total of eight diode heaters were placed in parallel, each 50 μm in length (8 μm p-doped) and 1.2-μm wide, placed 0.75 μm from the waveguide in the same plane.

To address the inherent challenge of nonlinear phase shift responses to applied voltage in diode heaters, the authors in Ref. 50 developed a linear response technique through the utilization of pulse-width modulation (PWM). By fixing the PWM signal amplitude above the diode heater's threshold voltage and modulating the signal's duty cycle, power delivery was linearized and controlled effectively. This diode heater configuration has been successfully applied to manage larger silicon photonic circuits, allowing for the digital control of matrix topologies comprising N rows and M columns by connecting $N \times M$ heaters.[53] Employing PWM signals and time-multiplexing across different channels, the system obviates the need for digital-to-analog converters, requiring only $M + N$ wires for comprehensive circuit control. An experimental demonstration controlling a 3×5 matrix with a 1×16 power splitter tree and 15 TOPSs via eight bond pads showcased this concept's effectiveness.[53]

For further acceleration of switching time, the pn junction can be directly integrated into the silicon waveguide, enhancing speed to the microsecond range[49] or even down to hundreds of nanoseconds.[48] However, this direct integration method results in a notable increase in the optical loss for the phase shifter, ~2 dB.[49]

4 Advanced Configurations

Advanced configurations in TOPSs aim to decouple the traditionally correlated lengths of the heater and the light path to enhance energy efficiency. This approach is characterized by extending the light-path length while maintaining the heater's length constant, thereby facilitating a greater phase shift for the same level of power consumption. The primary limitation of this strategy, however, lies in the requirement for larger device footprints to significantly reduce power consumption.

4.1 Folded Waveguides

Folded waveguides provide a straightforward method to extend the waveguide path length. By folding the silicon waveguide multiple time beneath the heater, for example, in a spiral configuration [illustrated in Figs. 5(a) and 5(b)], significant increases in path length can be achieved. Densmore et al.[54] reported the fabrication of a waveguide spiral comprising a total of 59 folds. To mitigate coupling, the separation between adjacent waveguides was maintained at 2 μm. A meander Cr/Au heater, separated from the photonic spiral by a 1.5-μm-thick SiO$_2$ layer, facilitated a temperature change $\Delta T_\pi = 0.67$°C across an active length of 6.3 mm for the TM polarization, resulting in a power consumption of ~6.5 mW.[54] When compared with a phase shifter employing a straight waveguide, the folded configuration demonstrated a fivefold reduction in power consumption (from 36 mW). The switching time was observed to be 14 μs, constrained by the thickness of the SiO$_2$ cladding surrounding the waveguide. Employing varying widths between adjacent waveguides can further mitigate phase matching and subsequent coupling.[55] In addition, releasing the entire phase
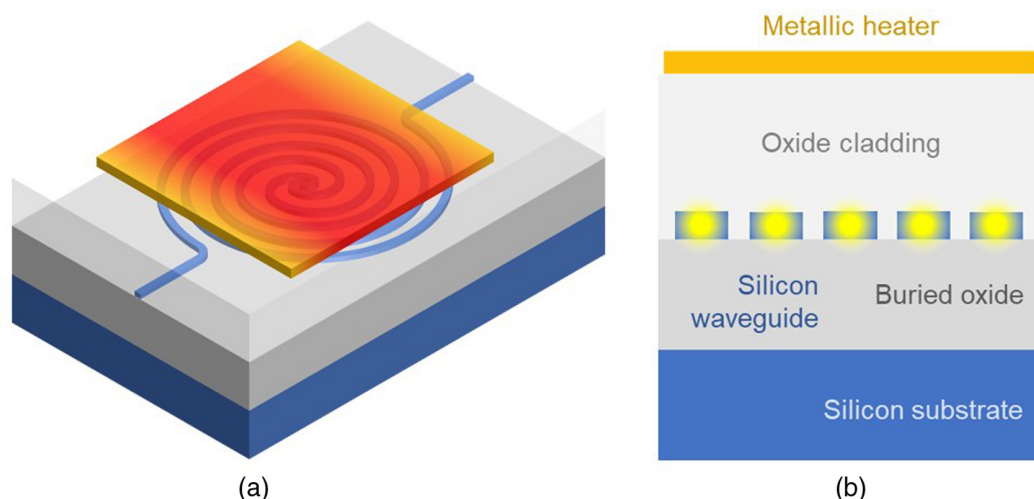
Fig. 5 (a) Illustration of a TOPS using folded waveguides based on a spiral waveguide with a wide heater on top. (b) Cross section of the folded TOPS. The folded waveguide needs to be designed to avoid cross-coupling between adjacent waveguides.

shifter structure can minimize power consumption to as low as 0.095 mW, albeit at the cost of a prolonged switching time of ∼1 ms (Table 4).

Additional optimization in folded TOPSs has been achieved through the incorporation of noncircular clothoid bends and the optimization of the heater's width and position.[56] This design facilitates a more efficient harnessing of generated heat. Peripheral waveguides are utilized to recollect residual heat energy, thereby enhancing the efficiency of the phase shifter without resorting to thermal isolation techniques such as air trenches or undercuts. This approach has demonstrated a power consumption of 2.56 mW and a switching speed of ∼35 μs. Subsequent research has yielded even higher performance, with a reported power consumption as low as 3 mW and a fast switching time of 11 μs.[57] In addition, optical losses in such devices have been minimized to 0.9 dB, achieved by introducing a slight offset at the junction between the bend and straight waveguide segments to mitigate the excitation of higher-order modes.

4.2 Multipass Waveguides

A recent innovative TOPS configuration relies on a multipass photonic architecture, enhancing the effective path length of light through a mode multiplexing approach. This strategy reduces the power consumption of the phase shifter while preserving high switching speed and, more importantly, broadband operation.[58] Indeed, while conventional resonant cavities enhance the effectiveness of phase shifters, this approach comes at the cost of narrowing the optical bandwidth. By contrast, the multipass strategy utilizes spatial mode multiplexing to circulate light multiple times through the phase shifter, with each pass converting the light to a higher-order orthogonal spatial mode. This method increases the effective path length without the need for a resonant cavity. It operates on the premise that the effective refractive indices of higher-order modes exhibit greater sensitivity to temperature changes due to their stronger dispersion. Thus, by integrating a TOPS into this multipass structure, light accumulates significant phase shifts from all passes.

The working principle is illustrated in Fig. 6: light is launched into the multipass structure in the TE_0 mode. As detailed in Ref. 58, the light is converted to the TE_1 mode upon exiting the multimode waveguide through a mode converter consisting of an adiabatic directional coupler. The TE_1 mode then circulates within the multimode waveguide in the opposite direction. Subsequently, light exits the multimode waveguide to be converted into the TE_2 mode and is sent back to the

Table 4 Summary of advanced experimental TOPSs using folded waveguides and metallic heaters in SiPh.

Ref.	Structure	Number of folds	Loss (dB)	P_π (mW)	Switching time (μm)[a]	FOM (mW μs)	Length (μm)
54	MZI	59	∼6[b]	∼6.5	∼14	∼91	∼13000
55	MZI	9	2.9[b]	4.2[c]/0.095[d]	65[c]/1200[d]	237[c]/114[d]	2900
56	MZI	14	1.23	2.56	35	89.6	2300
57	MZI	22	0.9	3	11	33	1876

N/A, not available; MZI, Mach–Zehnder interferometer.

[a]We consider the limiting switching speed of the switch in the case that the value of the phase shifter is not reported, i.e., the highest value between the rise and fall time constants.

[b]The value corresponds to the entire switching device. The optical loss of the phase shifter is not reported.
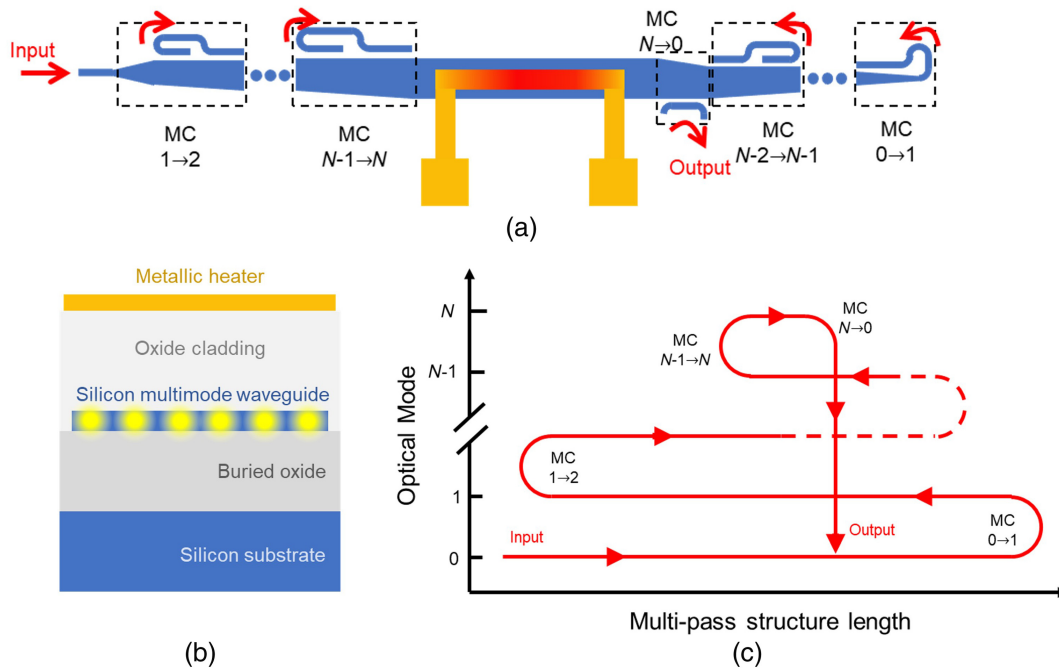
[c]With air trenches.

[d]With undercut.

Fig. 6 (a) Illustration of a TOPS utilizing a multimode waveguide where light is recycled N times through a multipass structure, demonstrating how power consumption decreases as the number of passes increases. (b) Cross section of the TOPS within the multimode waveguide. (c) Depiction of optical mode conversion as a function of the multipass structure's length. Light enters the structure in the fundamental mode and, after N passes, is converted to the Nth-order mode before being output from the structure and reverted to the fundamental mode.

multimode waveguide in the forward direction, and the process continues. Ultimately, the fundamental TE_0 mode is outputted from the structure.

This design was experimentally realized with a 360-μm-long Pt heater placed atop the multimode waveguide and separated by an intermediate 1-μm-thick SiO_2 layer. The device exhibited a switching time of 6.5 μs. Interestingly, the number of passes does not influence the device's switching time but does affect power consumption and optical loss. The effective path length—and consequently, the optical loss—increases with the number of passes due to the greater number of adiabatic couplers involved. For a three-pass phase shifter, the power consumption and insertion loss were measured at 4.6 mW and 1.2 dB, respectively. Increasing the passes to seven resulted in reduced power consumption, down to 1.7 mW, albeit with an elevated loss of almost 5 dB.

5 Other Phase Shifter Mechanisms and Technologies

In addition to leveraging the silicon thermo-optic effect, various mechanisms and technologies have been proposed to address the inherent limitations of TOPSs, including energy consumption, switching speed, and device footprint. Table 5 provides a comprehensive summary of both established and emerging electro-optical phase shifter technologies within the realm of SiPh.

5.1 Silicon Plasma-Dispersion Effect

The plasma-dispersion effect in silicon offers a well-established approach for implementing phase shifters. The underlying physical phenomenon is inherently rapid (on the order of

Table 5 Comparison of mainstream and emerging electro-optic technologies for implementing phase shifters in SiPh.

Technology	Insertion loss	Static power consumption	Switching time	Footprint	Manufacturability
Silicon TOPS	Ultralow (<1 dB)	Very high (>mW)	Very slow (> μs)	Large (>100 μm)	Excellent
Silicon PDE	High (>1 dB)	Moderate (> μW)	Very fast (<ns)	Very large (~mm)	Excellent
MEMS	Low (~1 dB)	Ultralow (~nW)	Slow (~μs)	Compact (~100 μm)	Good
Plasmonics	Very high (>5 dB)	Ultralow (~nW)	Ultrafast (~ps)	Ultracompact (~μm)	Limited
Ferroelectrics	Ultralow (<1 dB)	Ultralow (~nW)	Ultrafast (~ps)	Very large (~mm)	Limited
PCMs	Low (~1 dB)	Zero	Slow (~μs)	Ultracompact (~μm)	Limited

TOPS, thermo-optic phase shifter; PDE, plasma-dispersion effect.

hundreds of picoseconds) and can be realized through n-/p-doping of the silicon waveguide, utilizing the same fabrication processes available in microelectronic CMOS foundries.[59,60] In addition, the power consumption associated with such phase shifters is moderately low, typically in the microwatt range. However, these devices face two primary limitations. First, the plasma-dispersion effect alters both the real and imaginary components of the silicon refractive index,[61] leading to relatively high optical losses (>1 dB) in these phase shifters. Second, the refractive index change induced is minimal (on the order of 10^{-5}), necessitating large device footprints (on the scale of millimeters) to achieve significant phase shifts.[62–67]

To mitigate the issue of large footprints, resonant structures such as MRRs have been explored. However, these solutions introduce their own set of challenges, including high sensitivity to external thermal fluctuations and a limited operational bandwidth.[68–73]

5.2 Silicon Microelectromechanical Systems (MEMSs)

Over recent decades, silicon MEMS technology has achieved maturity, offering promising avenues for mechanical devices in photonics. MEMS-based phase shifters are known for their low optical loss (~1 dB), high energy efficiency, and compact footprints.[74–79] These mechanical devices function by altering the modal cross section of a suspended silicon waveguide through geometrical adjustments, facilitated by a MEM actuator. The application of a voltage bias between the movable shuttle and a fixed, anchored electrode generates an attractive force within the actuator. This force diminishes the gap between the sets of teeth, causing displacement of the free-hanging shuttle. Consequently, a phase shift is achieved due to changes in the effective refractive index of the guided mode, resulting from this geometrical tuning. The induced optical losses are minimal, primarily originating from optical mismatches caused by structural transitions.

The primary challenges associated with MEMS-based phase shifters include their switching speed (ranging from ~0.1 to 1 MHz), the relatively high driving voltage (exceeding 20 V), and the complexity of fabrication. Although MEMS technology is compatible with microelectronic industry manufacturing standards, the fabrication processes involved are intricate.

5.3 Plasmonics

The synergistic combination of nonlinear polymers with the high optical confinement afforded by plasmonics presents a promising avenue for the development of highly energy-efficient, ultrafast, and ultracompact phase shifters.[80–83] Nonetheless, a significant challenge of this approach is the very high optical loss, typically exceeding 5 to 10 dB, which stands as a principal limitation. In addition, the reliance on non-CMOS-compatible metals such as Au hinders the mass production of plasmonic devices. The long-term reliability and stability of the organic polymers used also necessitate further investigation.[84]

To address these challenges, TCOs emerge as promising candidates for new low-loss and CMOS-compatible plasmonic devices.[85–87] Notably, the significant free-carrier dispersion effect of ITO has been exploited to realize subwavelength-long phase shifters capable of subnanosecond switching speeds. This is achieved by electrostatically tuning the ITO carrier concentration close to, but not within, the high-loss epsilon-near-zero plasmonic region.[88] Despite these advancements, further

optimization is required, as the insertion loss associated with these devices remains substantial (>5 dB).

5.4 Ferroelectrics

Ferroelectric materials are recognized for their capacity to enable high-performance electro-optic devices by harnessing the Pockels effect. Unlike silicon, which lacks the Pockels effect due to its material symmetry, ferroelectrics offer ultrafast operational speeds (on the order of picoseconds) without contributing to optical loss. In recent years, various platforms have been proposed to utilize these distinctive properties for the development of ferroelectric-based phase shifters, ensuring compatibility with silicon photonic devices. Predominantly, these efforts have centered around lithium niobate (LN), a material with a longstanding history in commercial fiber-based electro-optic modulators.[89,90] Innovations in phase-shifting devices have led to the demonstration of both ultralow loss, ultrafast standalone LN thin films,[91] and hybrid LN/Si phase shifters,[92] noted for their high energy efficiency (less than pJ).

Alternatively, barium titanate (BTO) has emerged as a ferroelectric material with a Pockels coefficient significantly higher than that of LN (923 versus ~30 pm/V),[93,94] paving the way for experimental demonstrations of BTO/Si phase-based devices.[95–100] Recent advancements include the development of a multilevel nonvolatile phase shifter based on BTO/Si.[101] The direct growth of BTO on silicon highlights its potential for monolithic integration with electronic circuits and mass manufacturing within silicon photonic platforms. Furthermore, wafer-scale production has also been showcased in standalone LN on insulator[102] and LN on silicon nitride through heterogeneous integration.[103]

5.5 Phase-Change Materials (PCMs)

PCMs are distinguished by their dramatic optical refractive index change, facilitating the development of photonic devices with ultracompact footprints spanning only a few micrometers. The predominant PCMs utilized in photonics are chalcogenides,[104] capable of nonvolatile transitions between amorphous and crystalline states. This attribute may significantly decrease power consumption, as no static power is needed to maintain the material state.[105] State switching is typically achieved by locally heating the PCM through photothermal excitation with optical pulses or joule heating via microheaters,[104] leading to comparatively slower switching time (on the order of microseconds). Among various chalcogenide compounds, $Ge_2Sb_2Te_5$ (GST) has been extensively used.[106] However, GST's high optical absorption in both material states positions it as an ideal candidate for absorption-based devices such as optical memories[107,108] but limits its use in phase-based devices. Conversely, alloys such as $Ge_2Sb_2Se_4Te_1$ (GSST), Sb_2S_3, and Sb_2Se_3 show minimal or negligible optical absorption at telecom wavelengths.[107,109–116] In this regard, Sb_2Se_3/Si phase shifters have achieved an insertion loss of merely 0.36 dB with phase modulation up to $0.09\pi/\mu m$.[107]

However, the long-term reliability and endurance of PCMs in photonics remain challenging, attributed to material property degradation after numerous switching cycles.[117] Reversible switching operation up to only 10^4 cycles has been recently demonstrated in a Sb_2Se_3/Si phase-shifter device.[118] Thus, the application of PCMs in phase shifters might be confined to scenarios not demanding extensive cycling over time.

6 Conclusions and Prospects

In this review, a comprehensive overview of the current landscape of PIC technology is based on TOPSs. It has examined the most relevant heater technologies and advanced waveguide-heater configurations, highlighting the prevalent use of metallic heaters as the standard in SiPh due to their compatibility with CMOS foundry processes. Despite their widespread adoption, metallic heaters have been criticized for their high power consumption and slow response time. An alternative strategy, involving the release of the silicon waveguide, has been shown to significantly reduce power consumption, albeit at the cost of device speed.

The exploration of transparent materials, such as graphene and TCOs, offers promising avenues for enhancing performance by enabling closer placement of the heater to the waveguide. Nevertheless, the literature on these innovative approaches remains limited, underscoring a need for further investigation, particularly regarding their practical application and integration into the silicon photonic foundry fabrication processes.

Doping the silicon waveguide emerges as a preferable option for phase shifters requiring swift operation and minimal power consumption, as it facilitates internal heat generation within the waveguide. However, this method introduces optical losses due to free carriers. In addition, its application is confined to silicon waveguides, precluding its adoption in other photonic platforms, such as silicon nitride.

Addressing these open questions and challenges is crucial for advancing the field of TOPSs in PICs. Future efforts should aim at demonstrating the practical applications of these technologies and exploring their integration into standard fabrication processes, thereby paving the way for more efficient, faster, and versatile photonic devices.

Advanced waveguide-heater configurations present a promising avenue to augment the capabilities of conventional TOPS schemes. While existing implementations predominantly utilize metal heaters, the exploration of alternative materials, such as those based on transparent heaters, holds the potential to further capitalize on the advantages offered by these configurations. Notably, advanced approaches, including folded waveguides and light recycling, aim at minimizing power consumption without adversely affecting switching speed and optical bandwidth. This contrasts with strategies involving released waveguides, where power efficiency improvements often come at the cost of reduced operational speed.

A critical challenge associated with these advanced configurations is the inverse relationship between power consumption reduction and the TOPS footprint. In scenarios demanding high device density, such as in the deployment of deep-neural networks, the increased footprint could impose significant constraints. Consequently, there is a pressing need for novel strategies that concurrently optimize speed, power efficiency, and device compactness. Such developments would not only overcome existing limitations but also enable broader application of TOPSs in densely packed PICs.

This review also has explored various alternative mechanisms and technologies for phase shifters, each presenting unique advantages, limitations, and potential application scopes. The silicon plasma dispersion effect offers significantly faster operation speeds (lower than nanoseconds) while retaining fabrication compatibility with CMOS foundries. However, this approach incurs moderate insertion losses (>1 dB) and necessitates millimeter-scale footprints due to free-carrier effects and the inherently weak modulation mechanism.

Hybrid ferroelectric-SiPh platforms, utilizing materials such as LN or BTO, propose an avenue for ultralow loss (<1 dB) phase shifters capable of ultrafast speeds (on the order of picoseconds). Despite these advantages, their millimeter-long footprints may limit their applicability in densely integrated systems.

MEMS-based phase shifters emerge as a compact alternative (~100 μm), featuring low optical losses and ultralow power consumption (in the nanowatt range). Their operation, predicated on the mechanical displacement of released silicon waveguides via an external electric field, leverages CMOS-compatible fabrication processes. Nonetheless, the slow operational speeds (on the order of microseconds) and the necessity for high voltages, which are incompatible with standard CMOS voltages, pose significant drawbacks.

Plasmonic phase shifters have demonstrated potential for energy-efficient and ultrafast operation within the ultracompact footprints. The primary challenge for plasmonics lies in their very high optical losses (>5 dB), constraining scalability and suitability for certain applications, such as quantum optics.

PCMs stand out for applications requiring ultracompact devices or benefiting from nonvolatile phase tuning, offering the advantage of zero static energy consumption. However, the principal challenge for PCMs is ensuring long-term stable operation across numerous switching cycles, a critical requirement for many applications.

In summary, silicon's relatively high thermo-optic coefficient, alongside the potential for negligible insertion losses, positions thermal tuning as the most versatile and widely applicable approach in the vast array of integrated photonic applications, spanning fields from computing and quantum technologies to artificial intelligence. The choice of TOPS optimization strategy and configuration will inevitably be guided by the specific requirements of each application, considering the inherent trade-offs among power consumption, speed, and ease of fabrication. Consequently, additional research efforts are crucial for overcoming these challenges. Emerging technologies that offer alternative methods for implementing integrated phase shifters within the SiPh platform present a promising avenue for superseding traditional TOPSs. However, the determination of which technology will ultimately be embraced by existing CMOS foundries remains an open question, underscoring the dynamic and evolving nature of this field.

Disclosures

The authors declare no conflicts of interest.

Code and Data Availability

Data sharing is not applicable to this article, as no new data were created or analyzed.

References

1. S. Y. Siew et al., "Review of silicon photonics technology and platform development," *J. Lightwave Technol.* **39**, 4374–4389 (2021).
2. N. Margalit et al., "Perspective on the future of silicon photonics and electronics," *Appl. Phys. Lett.* **118**, 220501 (2021).
3. S. Shekhar et al., "Roadmapping the next generation of silicon photonics," *Nat. Commun.* **15**, 751 (2024).
4. Z. Xiao et al., "Recent progress in silicon-based photonic integrated circuits and emerging applications," *Adv. Opt. Mater.* **11**, 2301028 (2023).
5. Y. Zhang and J. Liu, "Prediction of overall energy consumption of data centers in different locations," *Sensors* **22**, 3704 (2022).
6. D. J. Thomson et al., "50-Gb/s silicon optical modulator," *IEEE Photonics Technol. Lett.* **24**, 234–236 (2012).
7. C. Xiong et al., "Monolithic 56 Gb/s silicon photonic pulse-amplitude modulation transmitter," *Optica* **3**, 1060 (2016).
8. X. Zhang et al., "A large-scale microelectromechanical-systems-based silicon photonics LiDAR," *Nature* **603**, 253–258 (2022).
9. N. C. Harris et al., "Quantum transport simulations in a programmable nanophotonic processor," *Nat. Photonics* **11**, 447–452 (2017).
10. C. Dhote, A. Singh, and S. Kumar, "Silicon photonics sensors for biophotonic applications—a review," *IEEE Sens. J.* **22**, 18228–18239 (2022).
11. M. Lipson, "The revolution of silicon photonics," *Nat. Mater.* **21**, 974–975 (2022).
12. W. Bogaerts et al., "Programmable photonic circuits," *Nature* **586**, 207–216 (2020).
13. J. Sun et al., "Large-scale nanophotonic phased array," *Nature* **493**, 195–199 (2013).
14. Y. Shen et al., "Deep learning with coherent nanophotonic circuits," *Nat. Photonics* **11**, 441–446 (2017).
15. D. M. Kita et al., "High-performance and scalable on-chip digital Fourier transform spectroscopy," *Nat. Commun.* **9**, 4405 (2018).
16. G. Cocorullo and I. Rendina, "Thermo-optical modulation at 1.5 μm in silicon etalon," *Electron. Lett.* **28**, 83–85 (1992).
17. J. Komma et al., "Thermo-optic coefficient of silicon at 1550 nm and cryogenic temperatures," *Appl. Phys. Lett.* **101**, 41905 (2012).
18. M. Bahadori et al., "Thermal rectification of integrated micro-heaters for microring resonators in silicon photonics platform," *J. Lightwave Technol.* **36**, 773–788 (2018).
19. M. Jacques et al., "Optimization of thermo-optic phase-shifter design and mitigation of thermal crosstalk on the SOI platform," *Opt. Express* **27**, 10456 (2019).
20. J. Parra et al., "Ultra-low loss hybrid ITO/Si thermo-optic phase shifter with optimized power consumption," *Opt. Express* **28**, 9393 (2020).
21. R. Espinola et al., "Fast and low-power thermooptic switch on thin silicon-on-insulator," *IEEE Photonics Technol. Lett.* **15**, 1366–1368 (2003).
22. J. Xia et al., "Low power 2 × 2 thermo-optic SOI waveguide switch fabricated by anisotropy chemical etching," *Opt. Commun.* **232**, 223–228 (2004).
23. T. Chu et al., "Compact 1 × N thermo-optic switches based on silicon photonic wire waveguides," *Opt. Express* **13**(25), 10109 (2005).
24. P. Dong et al., "Low power and compact reconfigurable multiplexing devices based on silicon microring resonators," *Opt. Express* **18**, 9852 (2010).
25. Y. Shoji et al., "Low-crosstalk 2 × 2 thermo-optic switch with silicon wire waveguides," *Opt. Express* **18**, 9071 (2010).
26. A. H. Atabaki et al., "Optimization of metallic microheaters for high-speed reconfigurable silicon photonics," *Opt. Express* **18**(17), 18312 (2010).
27. P. Sun and R. M. Reano, "Submilliwatt thermo-optic switches using free-standing silicon-on-insulator strip waveguides," *Opt. Express* **18**, 8406 (2010).
28. P. Dong et al., "Thermally tunable silicon racetrack resonators with ultralow tuning power," *Opt. Express* **18**, 20298 (2010).
29. J. Van Campenhout et al., "Integrated NiSi waveguide heaters for CMOS-compatible silicon thermo-optic devices," *Opt. Lett.* **35**, 1013 (2010).
30. Q. Fang et al., "Ultralow power silicon photonics thermo-optic switch with suspended phase arms," *IEEE Photonics Technol. Lett.* **23**, 525–527 (2011).
31. Q. Fang et al., "High efficiency ring-resonator filter with NiSi heater," *IEEE Photonics Technol. Lett.* **24**, 350–352 (2012).
32. A. H. Atabaki et al., "Sub-100-nanosecond thermal reconfiguration of silicon photonic devices," *Opt. Express* **21**, 15706 (2013).
33. A. Masood et al., "Fabrication and characterization of CMOS-compatible integrated tungsten heaters for thermo-optic tuning in silicon photonics devices," *Opt. Mater. Express* **4**, 1383 (2014).
34. B. Pant et al., "Study into the spread of heat from thermo-optic silicon photonic elements," *Opt. Express* **29**, 36461 (2021).
35. L. Yu, D. Dai, and S. He, "Graphene-based transparent flexible heat conductor for thermally tuning nanophotonic integrated devices," *Appl. Phys. Lett.* **105**, 251104 (2014).
36. D. Schall et al., "Infrared transparent graphene heater for silicon photonic integrated circuits," *Opt. Express* **24**(8), 7871 (2016).
37. S. Yan et al., "Slow-light-enhanced energy efficiency for graphene microheaters on silicon photonic crystal waveguides," *Nat. Commun.* **8**, 14411 (2017).
38. Z. Xu et al., "Ultra-compact tunable silicon nanobeam cavity with an energy-efficient graphene micro-heater," *Opt. Express* **25**, 19479 (2017).
39. A. Dash et al., "Carbon-nanotube-on-waveguide thermo-optic tuners," *Opt. Lett.* **43**, 5194 (2018).
40. D. Oz et al., "Optically transparent and thermally efficient 2D MoS_2 heaters integrated with silicon microring resonators," *ACS Photonics* **10**, 1783–1794 (2023).
41. W. Tong et al., "An efficient, fast-responding, low-loss thermo-optic phase shifter based on a hydrogen-doped indium oxide microheater," *Laser Photonics Rev.* **17**, 2201032 (2023).
42. A. A. Balandin et al., "Superior thermal conductivity of single-layer graphene," *Nano Lett.* **8**, 902–907 (2008).
43. L. Yu et al., "Thermally tunable silicon photonic microdisk resonator with transparent graphene nanoheaters," *Optica* **3**, 159 (2016).
44. M. Geis et al., "Submicrosecond submilliwatt silicon-on-insulator thermooptic switch," *IEEE Photonics Technol. Lett.* **16**, 2514–2516 (2004).
45. M. R. Watts et al., "Adiabatic thermo-optic Mach-Zehnder switch," *Opt. Lett.* **38**, 733 (2013).
46. N. C. Harris et al., "Efficient, compact and low loss thermo-optic phase shifter in silicon," *Opt. Express* **22**, 10487 (2014).
47. D. Patel et al., "A 4 × 4 fully non-blocking switch on SOI based on interferometric thermo-optic phase shifters," in *Opt. Interconnects Conf.*, IEEE, Vol. 5, pp. 104–105 (2014).
48. X. Li et al., "Fast and efficient silicon thermo-optic switching based on reverse breakdown of pn junction," *Opt. Lett.* **39**, 751 (2014).
49. X. Wang et al., "Wide-range and fast thermally-tunable silicon photonic microring resonators using the junction field effect," *Opt. Express* **24**, 23081 (2016).
50. A. Ribeiro and W. Bogaerts, "Digitally controlled multiplexed silicon photonics phase shifter using heaters with integrated diodes," *Opt. Express* **25**, 29778 (2017).
51. M. Mendez-Astudillo et al., "Compact thermo-optic MZI switch in silicon-on-insulator using direct carrier injection," *Opt. Express* **27**, 899 (2019).

52. T. Kita and M. Mendez-Astudillo, "Ultrafast silicon MZI optical switch with periodic electrodes and integrated heat sink," *J. Lightwave Technol.* **39**, 5054–5060 (2021).

53. A. Ribeiro et al., "Column-row addressing of thermo-optic phase shifters for controlling large silicon photonic circuits," *IEEE J. Sel. Top. Quantum Electron.* **26**, 1–8 (2020).

54. A. Densmore et al., "Compact and low power thermo-optic switch using folded silicon waveguides," *Opt. Express* **17**, 10457 (2009).

55. K. Murray et al., "Dense dissimilar waveguide routing for highly efficient thermo-optic switches on silicon," *Opt. Express* **23**, 19575 (2015).

56. S. Chung, M. Nakai, and H. Hashemi, "Low-power thermo-optic silicon modulator for large-scale photonic integrated systems," *Opt. Express* **27**, 13430 (2019).

57. H. Qiu et al., "Energy-efficient thermo-optic silicon phase shifter with well-balanced overall performance," *Opt. Lett.* **45**, 4806 (2020).

58. S. A. Miller et al., "Large-scale optical phased array using a low-power multi-pass silicon photonic platform," *Optica* **7**, 3 (2020).

59. G. T. Reed et al., "Silicon optical modulators," *Nat. Photonics* **4**, 518–526 (2010).

60. A. Rahim et al., "Taking silicon photonics modulators to a higher performance level: state-of-the-art and a review of new technologies," *Adv. Photonics* **3**, 1–23 (2021).

61. R. Soref and B. Bennett, "Electrooptical effects in silicon," *IEEE J. Quantum Electron.* **23**, 123–129 (1987).

62. A. Liu et al., "High-speed optical modulation based on carrier depletion in a silicon waveguide," *Opt. Express* **15**, 660 (2007).

63. D. Marris-Morini, et al., "Low loss and high speed silicon optical modulator based on a lateral carrier depletion structure," *Opt. Express* **16**(1), 334 (2008).

64. F. Y. Gardes et al., "40 Gb/s silicon photonics modulator for TE and TM polarisations," *Opt. Express* **19**, 11804 (2011).

65. T. Baehr-Jones et al., "Ultralow drive voltage silicon traveling-wave modulator," *Opt. Express* **20**, 12014 (2012).

66. J. Ding et al., "Electro-optical response analysis of a 40 Gb/s silicon Mach-Zehnder optical modulator," *J. Lightwave Technol.* **31**, 2434–2440 (2013).

67. X. Xiao et al., "High-speed, low-loss silicon Mach–Zehnder modulators with doping optimization," *Opt. Express* **21**, 4116 (2013).

68. Q. Xu et al., "Micrometre-scale silicon electro-optic modulator," *Nature* **435**(7040), 325–327 (2005).

69. J. C. Rosenberg et al., "A 25 Gbps silicon microring modulator based on an interleaved junction," *Opt. Express* **20**, 26411 (2012).

70. D. Marris-Morini et al., "Low loss 40 Gbit/s silicon modulator based on interleaved junctions and fabricated on 300 mm SOI wafers," *Opt. Express* **21**, 22471 (2013).

71. S. Meister et al., "High-speed Fabry–Pérot optical modulator in silicon with 3-μm diode," *J. Lightwave Technol.* **33**, 878–881 (2015).

72. R. Dubé-Demers, S. LaRochelle, and W. Shi, "Ultrafast pulse-amplitude modulation with a femtojoule silicon photonic modulator," *Optica* **3**, 622 (2016).

73. J. Sun et al., "A 128 Gb/s PAM4 silicon microring modulator with integrated thermo-optic resonance tuning," *J. Lightwave Technol.* **37**, 110–115 (2019).

74. C. Errando-Herranz et al., "Low-power microelectromechanically tunable silicon photonic ring resonator add-drop filter," *Opt. Lett.* **40**, 3556 (2015).

75. M. W. Pruessner et al., "Broadband opto-electro-mechanical effective refractive index tuning on a chip," *Opt. Express* **24**, 13917 (2016).

76. H. Sattari et al., "Silicon photonic MEMS phase-shifter," *Opt. Express* **27**, 18959 (2019).

77. R. Baghdadi et al., "Dual slot-mode NOEM phase shifter," *Opt. Express* **29**, 19113 (2021).

78. T. Grottke et al., "Optoelectromechanical phase shifter with low insertion loss and a 13π tuning range," *Opt. Express* **29**, 5525 (2021).

79. P. Edinger et al., "Silicon photonic microelectromechanical phase shifters for scalable programmable photonics," *Opt. Lett.* **46**, 5671 (2021).

80. A. Melikyan et al., "High-speed plasmonic phase modulators," *Nat. Photonics* **8**, 229–233 (2014).

81. C. Haffner et al., "All-plasmonic Mach-Zehnder modulator enabling optical high-speed communication at the microscale," *Nat. Photonics* **9**, 525–528 (2015).

82. C. Haffner et al., "Low-loss plasmon-assisted electro-optic modulator," *Nature* **556**, 483–486 (2018).

83. W. Heni et al., "Plasmonic IQ modulators with attojoule per bit electrical energy consumption," *Nat. Commun.* **10**, 1694 (2019).

84. M. Xu and X. Cai, "Advances in integrated ultra-wideband electro-optic modulators [Invited]," *Opt. Express* **30**, 7253 (2022).

85. G. V. Naik, J. Kim, and A. Boltasseva, "Oxides and nitrides as alternative plasmonic materials in the optical range [Invited]," *Opt. Mater. Express* **1**, 1090 (2011).

86. G. V. Naik, V. M. Shalaev, and A. Boltasseva, "Alternative plasmonic materials: beyond gold and silver," *Adv. Mater.* **25**, 3264–3294 (2013).

87. W. Jaffray et al., "Transparent conducting oxides: from all-dielectric plasmonics to a new paradigm in integrated photonics," *Adv. Opt. Photonics* **14**, 148 (2022).

88. R. Amin et al., "Sub-wavelength GHz-fast broadband ITO Mach–Zehnder modulator on silicon photonics," *Optica* **7**(4), 333 (2020).

89. Y. Qi and Y. Li, "Integrated lithium niobate photonics," *Nanophotonics* **9**, 1287–1320 (2020).

90. D. Zhu et al., "Integrated photonics on thin-film lithium niobate," *Adv. Opt. Photonics* **13**, 242 (2021).

91. C. Wang et al., "Nanophotonic lithium niobate electro-optic modulators," *Opt. Express* **26**, 1547 (2018).

92. M. He et al., "High-performance hybrid silicon and lithium niobate Mach-Zehnder modulators for 100 Gbit s-1 and beyond," *Nat. Photonics* **13**, 359–364 (2019).

93. S. Abel et al., "A strong electro-optically active lead-free ferroelectric integrated on silicon," *Nat. Commun.* **4**, 1671 (2013).

94. K. J. Kormondy et al., "Microstructure and ferroelectricity of $BaTiO_3$ thin films on Si for integrated photonics," *Nanotechnology* **28**, 075706 (2017).

95. P. Castera et al., "Influence of $BaTiO_3$ ferroelectric orientation for electro-optic modulation on silicon," *Opt. Express* **23**, 15332 (2015).

96. S. Abel et al., "A hybrid barium titanate–silicon photonics platform for ultraefficient electro-optic tuning," *J. Lightwave Technol.* **34**, 1688–1693 (2016).

97. F. Eltes et al., "A $BaTiO_3$-based electro-optic Pockels modulator monolithically integrated on an advanced silicon photonics platform," *J. Lightwave Technol.* **37**, 1456–1462 (2019).

98. J. E. Ortmann et al., "Ultra-low-power tuning in hybrid barium titanate-silicon nitride electro-optic devices on silicon," *ACS Photonics* **6**, 2677–2684 (2019).

99. S. Abel et al., "Large Pockels effect in micro- and nanostructured barium titanate integrated on silicon," *Nat. Mater.* **18**, 42–47 (2019).

100. F. Eltes et al., "An integrated optical modulator operating at cryogenic temperatures," *Nat. Mater.* **19**, 1164–1168 (2020).

101. J. Geler-Kremer et al., "A ferroelectric multilevel non-volatile photonic phase shifter," *Nat. Photonics* **16**, 491–497 (2022).

102. K. Luke et al., "Wafer-scale low-loss lithium niobate photonic integrated circuits," *Opt. Express* **28**, 24452 (2020).

103. L. Chang et al., "Heterogeneous integration of lithium niobate and silicon nitride waveguides for wafer-scale photonic integrated circuits on silicon," *Opt. Lett.* **42**, 803 (2017).

104. S. Abdollahramezani et al., "Tunable nanophotonics enabled by chalcogenide phase-change materials," *Nanophotonics* **9**, 1189–1241 (2020).
105. J. Parra et al., "Toward nonvolatile switching in silicon photonic devices," *Laser Photonics Rev.* **15**, 2000501 (2021).
106. Z. Gong et al., "Phase change materials in photonic devices," *J. Appl. Phys.* **129**, 030902 (2021).
107. C. Ríos et al., "Ultra-compact nonvolatile phase shifter based on electrically reprogrammable transparent phase change materials," *PhotoniX* **3**, 26 (2022).
108. X. Li et al., "Fast and reliable storage using a 5 bit, nonvolatile photonic memory cell," *Optica* **6**, 1 (2019).
109. Y. Zhang et al., "Broadband transparent optical phase change materials for high-performance nonvolatile photonics," *Nat. Commun.* **10**, 4279 (2019).
110. Q. Zhang et al., "Broadband nonvolatile photonic switching based on optical phase change materials: beyond the classical figure-of-merit," *Opt. Lett.* **43**, 94 (2018).
111. S. A. Vitale et al., "Phase transformation and switching behavior of magnetron plasma sputtered Ge$_2$Sb$_2$Se$_4$ Te," *Adv. Photonics Res.* **3**, 2200202 (2022).
112. M. Delaney et al., "A new family of ultralow loss reversible phase-change materials for photonic integrated circuits: Sb$_2$S$_3$ and Sb$_2$Se$_3$," *Adv. Funct. Mater.* **30**, 2002447 (2020).
113. Z. Fang et al., "Non-volatile reconfigurable integrated photonics enabled by broadband low-loss phase change material," *Adv. Opt. Mater.* **9**, 2002049 (2021).
114. Z. Fang et al., "Low-loss broadband nonvolatile 2×2 switch based on Sb$_2$Se$_3$ for programmable silicon photonics," in *Conf. Lasers and Electro-Opt.*, Optica Publishing Group, San Jose, California, p. STh4G.6 (2022).
115. Z. Fang et al., "Ultra-low-energy programmable non-volatile silicon photonics based on phase-change materials with graphene heaters," *Nat. Nanotechnol.* **17**, 842–848 (2022).
116. R. Chen et al., "Non-volatile electrically programmable integrated photonics with a 5-bit operation," *Nat. Commun.* **14**, 3465 (2023).
117. R. Chen et al., "Opportunities and challenges for large-scale phase-change material integrated electro-photonics," *ACS Photonics* **9**, 3181–3195 (2022).
118. X. Yang et al., "Non-volatile optical switch element enabled by low-loss phase change material," *Adv. Funct. Mater.* **33**, 2304601 (2023).

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