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Control of Integrated Circuit Patterning Variance, Part 3: Pattern Roughness, Local Uniformity, and Stochastic Defects

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Pattern variation due to stochastic processes is a significant problem for advanced semiconductor manufacturing. This variation can impact wafer patterning either quantitatively (CD uniformity, line-edge or linewidth roughness, edge placement error) or qualitatively (micro-bridges or breaks, closed or bridged contacts). Sources of stochastic variation include photo mask and lithography, as well as downstream processing such as etch, deposition, and cleans. While stochastic pattern variation is not a new problem, it becomes more challenging with smaller design rules where (1) feature roughness becomes an increasing percentage of the feature size, 10% to 20% in some cases, when (2) exposures of greater than 1 trillion features per wafer pass are expected to yield, and with (3) EUV lithography and its challenges of source power and throughput.

Integrated circuit (IC) patterning control addresses variance on multiple length scales. Longer length scales are typically characterized by critical dimension (CD), and pattern placement (mask registration, wafer alignment, and layer-to-layer centerline overlay), both of which are covered in previous special sections of JM3. Shorter length scale variability is characterized by line-edge roughness (LER), linewidth roughness (LWR), local CD uniformity (LCDU), pattern placement roughness, and stochastic defectivity, and is the focus of this special section. As the industry moves to sub-10 nm node design rules, the discrete nature of light due to shot noise (e.g. one contact may use as few as ~100 photons in an EUV exposure scenario) and the discrete nature of matter come into play. Even in cases where conventional continuum analysis would predict a sufficient process window, stochastic defects can occur due to the discrete nature of the light-matter interaction.

This year marks the 100th anniversary of the seminal paper by Walter Schottky on the study of the current fluctuations of vacuum tubes run at low currents, which he called the "shot effect." Burkhardt now provides an excellent new historical translation of that paper, originally published in 1918. Mack provides a 100-year historical perspective on what is now called shot noise, and its effect on understanding the impact of discrete particles or events in lithography.

Many of the papers in this special section focus on a diversity of perspectives on the metrology and characterization of LER and related effects. Fukuda et al. focus on edge detection, power spectral density (PSD) prediction, sampling strategy, and noise mitigation for SEM metrology of LER and LCDU. Reche et al. compare three different LER metrologies: CD SEM, optical critical dimension (OCD), and small angle x-ray scattering (SAXS). Wang et al. report on a high throughput review SEM to characterize a large volume of data related to stochastic and systematic effects over large and local scales. Lorusso et al. propose a standardized LWR measurement protocol in order to address the emerging stringent specs below 2 nm near term and below 1 nm in a few years. Takamasu et al. focus on reference metrology using focused ion beam techniques, as well as planar transmission electron microscope (TEM) methods. And finally, Constatoudis et al. cover topics of completeness and accuracy of LER characterization.

Another set of papers focuses on the process, simulation and mitigation of LER and related effects for EUV. Maas et al. look at metal-oxide-based nonchemically amplified resists (non-CARs) and investigate how the properties of these non-CARs impact LCDU. Mack looks at reducing roughness through lithographic and etch optimization, and the importance of roughness metrology to guide improvements. Gabor et al. investigate the statistics used for design-rule calculations and examine the impact of EUV lithography on sources of variation important for design-rule calculations. Bisschop et al. investigate stochastic effects in EUV lithography, including LCDU and stochastic failures, and ways to characterize and minimize those effects. Chen et al. describe a comprehensive investigation of mask impact on LWR. Bakaert et al. look at a novel approach to minimize the impact of defectivity of EUV masks. Naulleau et al. investigate CARs and the propagation of stochastic variability from both material and photon sources in EUV lithography. Rutigliani et al. use PSD analysis to understand LER and LWR and use it to guide EUV material stack selection.

In summary, this special section includes papers that present a diversity of ideas that address the technical challenges of semiconductor process development and manufacturing characterized by LER, LWR, LCDU, pattern placement

roughness, and stochastic defectivity. It is our intention that this collection of papers, in a refereed journal, will give a broad perspective on current challenges and future prospects. We would like to thank the authors for their excellent technical submissions and thoughtful responses to the reviewers' comments. Additionally, we'd like to thank the

reviewers for their hard work and thoughtful inputs, resulting in the excellent papers presented here. We'd also like to thank the editorial board of JM3 for giving us this opportunity to guest edit this special section, and to thank the staff of JM3 in making this special section a success.