REVIEW

All-optical photonic crystal logic gates for optical computing: an extensive review

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Abstract. Internet-based communication has become a major field, with a user base that is expanding day-by-day. The needs have overloaded the available bandwidth, and higher speed has become a mandatory requirement to satisfy the user demands and increased use of the internet. Therefore, there is a need for high-performance computers due to increasing dependence on computing technology. Optics is emerging as the best possible solution over electronics because it is capable of providing parallel data processing with fewer expenses and greater speed of more than 10,000 times faster than electronic computers. The main building block of optical computing is the all-optical logic gates, which are designed using different techniques. Different types of photonic crystal-based all-optical logic gates have been reviewed in detail by discussing the key characteristics and demonstrating the advantages over the previously available technologies (semiconductor optical amplifier and nonlinear waveguide) that are used to build all-optical logic gates. © *2020 Society of Photo-Optical Instrumentation Engineers (SPIE)* [DOI: 10.1117/1.OE.59.11.110901]

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1 Introduction

With the continuous advancement in technology, there has been a drastic computer evolution in different ways over the years. The first way of making a computer was mechanical methods (1623 to 1945).[1] In the earlier 17th century, scientists tried to make machines that could solve mathematical problems easily. There were several attempts made by several scientists, such as Gottfried Leibnitz, Wilhelm Schickhard, and Blaire Pascal, to design a calculator that was capable of performing addition, subtraction, multiplication, and division. George Schertz and Edward Schertz designed a 4-bit difference engine and made a machine that could process 15-digit numbers.[1] The US Census Bureau was one of the agencies that used the mechanical computer for punch card equipment for the census, which was drafted by Herman Hollerith from the company International Business Machines.[1]

Due to the large size, slow speed, low functionality, and complexity of mechanical computers, computer technology shifted toward the electronic computer. In the electronic computer, there were electronic switches in the form of vacuum tubes instead of the electromechanical relays in mechanical computers. The first attempt to make an electronic computer was by professor JV Atanaoff, who built a machine that solved partial differential equations. [1] The first computer in the world was designed by German pioneer Konrad Zuse, also known as the father of computer; he designed the architecture of the Z1 and Z3 computing machines in Berlin between 1936 and1941.[2] As time passed, research shifted toward making smaller electronic computers that have high speed, low complexity, and low heat dissipation. Therefore, electronic switches through vacuum tubes were replaced by diode and transistor technology, which has a switching time of $\sim 0.3\ \mu s$.[1,3] The first machine draft using this technology was TRADIC at Bell Laboratories in 1954. But the processing of transistor technology was still slow and only made for a particular purpose. To overcome the limitations of the diode and transistor technology,

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integrated circuits were introduced; these included IC's (semiconductor device with a large number of transistors on a single chip), semiconductor memories, and microprogramming and became a unique technique for efficiently designing complex processors. The first IC was based on small-scale integration circuits, which have around 10 devices per circuit; these further evolved to use medium scale integrated circuits that have up to 100 devices per chip.[1] In 1972, there was an evolution of technology with large-scale integration (1000 devices per chip) and very large-scale integration (VLSI—1000,000 devices per chip), which were used for the construction of electronic computers with the advantages of high speed of computation with accuracy, small size, and high endurance. The smallest dimension achieved using VLSI technology to date was 0.08 mm.[4]

But in today's world of internet and applications based on high bandwidth, such as internet television, multimedia, etc., there is a demand for computers with higher speed, lower complexity, smaller size, more accuracy, and less heat dissipation. To achieve these demands, optics is the best possible solution as it is a reliable and fast means of conveying information from one point to another. This is because a light beam can easily travel in free space without any cross talk.[4] Optics is an opportunity to go beyond the boundaries for ultrafast data transmission with fewer expenses and more reliability.[5–7] So, the optical computer is the best possible solution over the electronic computer as it performs multiple operations simultaneously and is capable of processing data 100,000 times faster.[4] High speed without heat dissipation is the other advantage of optics over electronics. Speed is the generally recommended advantage of optical computing. Electronics generally have two ways of handling complexity, i.e., the use of space or time, but optics provide a third way of fan-in and fan-out in which many independent beams may be modified by a single pixel in an optical processor.[4,8] Another parameter is heat dissipation in electronic devices because as speed increases, density decreases, according to Moore's law (doubling the number of transistors in 2 years), which is mitigated using optics. Another advantage of optics is that the signal is transmitted without the need to apply a voltage, in which generated light propagates by itself according to Maxwell's equations. Also, optical devices are compact, lightweight, and inexpensive to the manufacturer. By replacing electrons with photons, fiber optics, crystals, and thin films are used to build an optical computer, which will be 100 million times faster than today's available machines.

To build an optical computer, there is a requirement for a large variety of components, such as optical gates, optical switches, optical interconnects, and optical memory. In recent years, all-optical logic gates have been increasingly used due to their applications in ultrafast information processing[6] and ability to carry out different logical operations in the optical computing systems.[5] Therefore, the designing of the all-optical logic gates is the first step toward the realization of complex digital functionalities in optical computers. Earlier, electronic logic gates were used, but the maximum switching speed achieved was 50 ps for the average power of 0.5 mW per one switching.[9] The reason for this is the restricted capacitance of p-n junctions in semiconductor-based logic gates. Although today's available electronic logic gates are small, switching is still limited by interlinking capacitance; on the other hand, the switching speed of optical logic gates is in the femtosecond range[10] and limited only by the velocity of light passing through it. There are many different ways in which all-optical logic gates can be designed. The first method uses semiconductor optical amplifier (SOA), which exhibits strong gain due to changes in the refractive index. The first method to build all-optical logic gates was by introducing nonlinearity using one of the three techniques, i.e., cross-gain modulation,[10,11] cross-phase modulation,[11] and four-wave mixing.[12,13] In another method, SOA was used to design all-optical logic gates known as SOA-assisted interferometer-based gates.[14–43] But gates based on SOA suffer from many disadvantages, such as SOA-based devices that are limited by the slow carrier's recovery time of SOA, unstable gates due to polarization-sensitive, and the SOA Mach–Zehnder interferometer (MZI) method, which requires more than two SOAs and makes the system complicated by requiring the proper tuning of the filter for SOA with the assistance of optical fiber logic gates as, otherwise, detuning of the filter degrades the signal to noise ratio. Another method for designing all-optical logic gates uses nonlinear waveguides in which localized nonlinear media were utilized by changing the control power.[44–51] Nonlinear waveguide-based gates suffer from many disadvantages such as the requirement of high input signal power and polarization dependency, which creates challenges during manufacturing.

To overcome the disadvantages of the above techniques, we consider the only solution to be photonic crystal (PhC)-based all-optical logic gates. These are reviewed in this paper in detail and are further characterized into bandgap-based gates and nonbandgap-based gates. Mainly, parameters such as contrast ratio (CR), bit rate (Tb/s), area ($\mu m \times \mu m$), and threshold value have been compared and discussed.

2 PhC-Based Logic Gates

Photonic crystals (PhCs) are periodically structured dielectric or electromagnetic media that possess photonic bandgaps having frequency ranges through which light cannot propagate. PhC was introduced by John.[52] These are the crystals that affect the properties of photons, unlike semiconductor crystals that affect the property of electrons. Light has numerous advantages over the electrons as it can travel with greater speed in dielectric material than the electrons in metallic wire, and, the information-carrying capacity of light in the dielectric is higher than that of the electrons. Fiber-optic communication systems have bandwidth of the order of 1 THz, whereas electronic systems have bandwidth of the order of only a few hundred hertz. PhCs offer periodic dielectric media for the flowing of light, and these variations can be in different directions.[53] So, depending on the directions that a PhC can offer periodic variations in dielectric media, it is classified as follows:

- One-dimensional (1D) PhCs: Crystal structures that offer dielectric media variation only in one direction;
- Two-dimensional (2D) PhCs: Crystal structures that offer dielectric media variations in two directions;
- Three-dimensional (3D) PhCs: Crystal structures that offer dielectric media variations in three directions.

The 1D PhC is the type of crystals that offers periodic dielectric media variations only in one direction, as shown in Fig. 1(a).[53] The 1D PhCs have applications such as antireflection mirrors as the central rear mirror in vehicles, transparent TV screens, etc. However, applications of 1D PhCs are limited and cannot be used in building all-optical logic gates as this requires confinement of light, which can be achieved using 2D and 3D PhCs.

The 2D PhCs offer a periodic dielectric variation in two directions to the flow of light, as shown in Fig. 1(b).[53] These crystals are widely used in applications with different defects, such as self-collimated beam, Mach–Zehnder interferometer (MZI), multimode interference (MMI), interference, and nonlinear effects, to build all-optical logic gates as it provides a confinement facility from two directions.

The 3D PhC offers dielectric medium variations in all three dimensions, as shown in Fig. 1(c).[53] In comparison with the other types of PhCs, 3D PhCs are complex because they localize light at the center of the PhCs.

All of the PhC dielectric structures (1D, 2D, and 3D) exhibit the special property called photonic bandgap (PBG), which is analogous to the energy bandgap of crystalline atomic lattice.[53] The bandgap is a range of frequencies that are forbidden to propagate through the

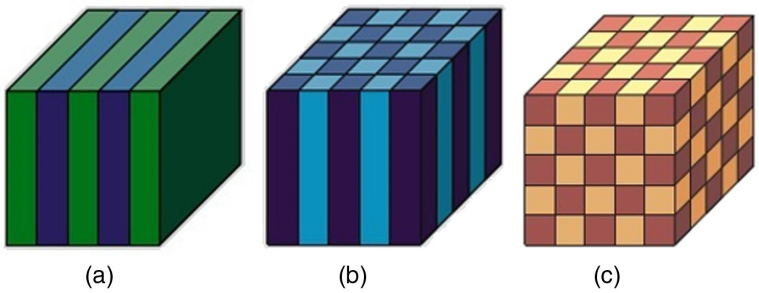

Fig. 1 Periodicity of photonic crystals: (a) periodicity in 1D, (b) periodicity in 2D, and (c) periodicity in 3D.

periodic crystal structures. Perfect bandgap can be only achieved using perfect symmetry in the PhC structure. Light of a certain wavelength can be made to travel through the crystal structure by introducing defects in the structure. With the help of a PBG, it can control the flow of photons or electromagnetic waves. All-optical logic gates are one of the important applications in the field of high data transmission, which can be achieved using 2D PhCs. Further, the PhC-based gates are divided into two types, i.e., bandgap-based gates and nonbandgap-based gates.

2.1 *Nonbandgap-Based All-Optical Logic Gates*

In nonbandgap-based PC gates, rather than finding the bandgap of the structures, the input beam of any wavelength is applied at the input, and a logic operation is performed using a self-collimated beam. In it, the incident light propagates along a specific direction in a structure without having diffraction. Total internal reflection (TIR) is the phenomenon used to build all-optical logic gates using a self-collimated beam. According to the relation $\theta >$ arc sin (n_L/n_H), where n_L represented the low refractive index and n_H represented the refractive index, TIR occurs when the angle of incidence is greater than the critical angle. Let us clarify the self-collimated beam using the structure in Fig. 2.

In Ref. 54, a device for the photonic-integrated circuit (PIC) based on a self-collimated beam in a 2D PhC was proposed. The device was relevant to building optical switches and logic gates, which were key components of a PIC. Square lattice geometry was used to design the structure with Si rods in air. In the proposed structure, radii and dielectric constant chosen for the structure were $r = 0.35a$ and $\varepsilon = 12.0$. To transmit the beam, a line defect was created in the $\Gamma - x$ direction by reducing the size of the 25 holes to $0.274a$. The principle behind this was to create a low refractive index medium so that one part of the beam continued to propagate and the other was reflected, which shows the presence of transmitted beams and reflected beams for the input signals, to produce the phase shift at the output. The OR and XOR gate structure was proposed by varying the phase difference between the reflected beam and transmitted beam. When the phase difference between the input beams, as shown in Fig. 2, was $2k\pi + \pi/2$, output O_1 operated as an OR gate and O_2 as an XOR gate. On the other hand, when the phase difference was $2k\pi - \pi/2$ due to having a phase difference of $-\pi/2$ between the input beams, O_1 acted as an XOR gate and O_2 as an OR gate. The frequency range selected for the device was 0.188 to 0.199 (a/λ), and the highest extinction ratio achieved was 17 dB.

A self-collimation waveguide that was polarization insensitive was proposed by Hou et al.,[55] as shown in Fig. 3. The structure was designed using square lattice geometry in 2D PhC with air holes in a silicon background. The proposed design was mainly focused on two parameters, i.e., inner rod radius r and outer ring radius R, so that the self-collimation band was shifted to a lower frequency. The first case taken was when R was fixed at $0.45a$ and r was varied from $0a$ to $0.3a$. In the second case, r was fixed at $0a$ and the outer ring radius R was varied from $0.25a$ to $0.48a$. The result show that, by increasing the inner rod radius r and decreasing outer ring radius R, self-collimation was shifted toward a lower frequency. The bandwidth achieved in this high dielectric contrast system was up to 102.9 nm.

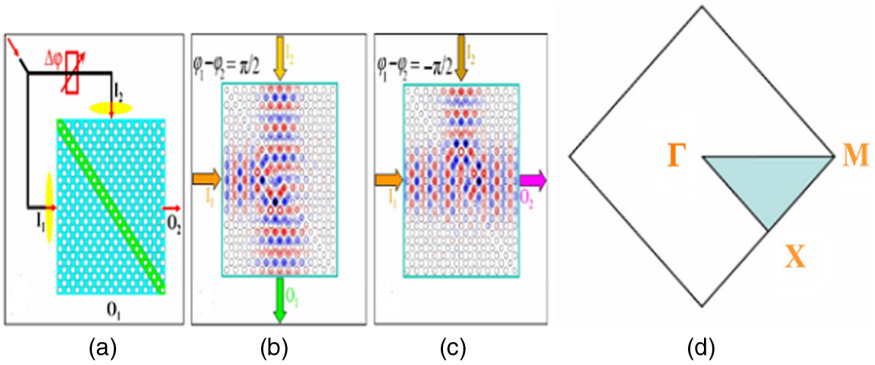

Fig. 2 (a) The structure for OR and XOR logic gates with phase shifter (b) when phase difference is $\pi/2$, (c) when phase difference is $-\pi/2$, and (d) different directions in the square lattice structure.

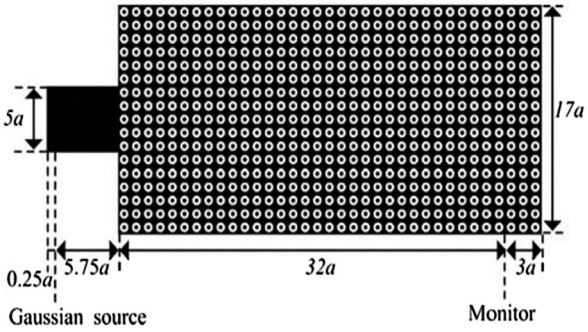

Fig. 3 Structure for self-collimation waveguide based on photonic crystal, where white is the outer ring having radius R and black is the inner ring with radius r.

The all-optical logic gate structure of the NOT, OR, AND, and XOR gates based on the self-collimated beam was proposed by Fan et al.[56] for the application of the PIC. The structure was built on 2D square lattice geometry with air holes in Si as the background material. The radius of the holes was $0.3a$, where a is the lattice constant with a value of 0.4185 μm, and the dielectric constant of background material was 11.56. According to the proposed structure in Fig. 4, two line defects, which corresponded to inputs A and B, were introduced; they operated at a wavelength of 1550 nm and had two splitters S_1 and S_2 designed by varying the rod radius from 0 to $0.5a$. According to the phenomenon of the self-collimated beam, the structure was designed based on the phase difference between the input signals. In Fig. 4, when there was light input at the input port A and the reference port B of the same intensities, there was partial reflectance of the input beam from A while the beam from B was totally reflected, and when these beams interfere with each other, there was an output at the port I that depended on the phases at the inputs and interfered constructively or destructively.

In Ref. 57, the self-collimated beam-based AND, NAND, XNOR, and NOR logic gates were proposed. The structure was designed using triangular lattice geometry in which rods were made of Si material in an air background. The radius of the holes selected was 105 nm with the lattice constant (a) of 302 nm. Two line defects were created in the $\Gamma - x$ direction by decreasing the radius of 15 rods, and the distance maintained between them was $10a$. After that, the defect radius was varied, and it was found that when the defect rod radius was about 83 nm, there was an equal distribution of transmitting and reflecting power. In another case, when the defect rod radius was greater than 83 nm, the phase difference of $-\pi/2$ was achieved between transmitted and reflected power that otherwise had a phase difference of $+\pi/2$. As seen from Fig. 5, there were two input signals (I_1 and I_2) sent at defect 1 and a reference signal (I_{ref}) at defect 2, which operate at 1555.1 nm. For the proposed structure to work as an AND gate, the values of the input signals and the reference signal taken were $2\,I_o$ and $0.5\,I_o$, respectively. Depending on the phase difference given at the input with respect to the reference signal, it interferes constructively or destructively at defect 2. When there was no signal at the input, I_{ref} ($0.5\,I_o$) at defect 2 was equally divided, and if either signal was high, it was equally divided by defect 1, as its reflected part interfered with defect 2, and the output intensity of $0.25\,I_o$ was detected at the output, which was considered "logic 0." The value greater than $0.25\,I_o$ was considered "logic 1."

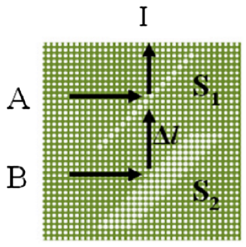

Fig. 4 Structure of NOT and AND gates with Δl as distance between two splitters and l as output.

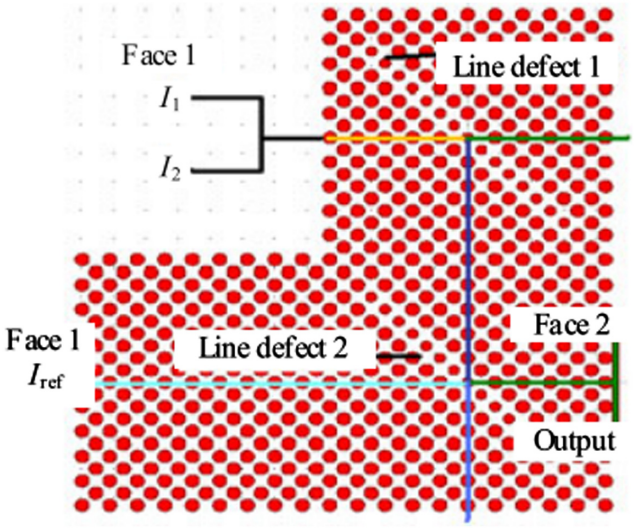

Fig. 5 Schematic of AND, NAND, XNOR, and NOR logic gates using self-collimated beam.

In the case of the NAND gate, the only difference was that the input and reference signals were set to $I_1 = I_2 = I_{ref} = 2I_o$ and the output was observed; for the NOR logic gate, the combination of input taken was $I_1 = I_2 = I_{ref} = I_o$. Another logic gate proposed was the XNOR logic gate in which inputs chosen were $2I_o$ and $I_{ref} = I_o$. The highest CR achieved was 6 dB.

In Ref. 58, a structure using a self-collimated beam and splitting phenomenon in 2D PhC was proposed. The structure was built using Si ($n = 3.52$) rods in an air background aligned in triangular lattice geometry. In the proposed design, two line defects were created in the $\Gamma - x$ direction by changing the defect hole radius to $0.275a$ (where a was a lattice constant with the value of 365 nm) while the surrounding hole area radius was $0.35a$. The radius of the defect was smaller as it produced a phase difference of $+\pi/2$ between the transmitted and reflected beams. The two input ports I_1 and I_2 and two output ports, O_1 for the OR gate and O_2 for the XOR gate, are shown in Fig. 6. When input with a phase difference of $+\pi/2$ was applied at I_1, it interfered with I_2 at the second line defect, which produced constructive interference at O_1 and destructive interference at O_2.

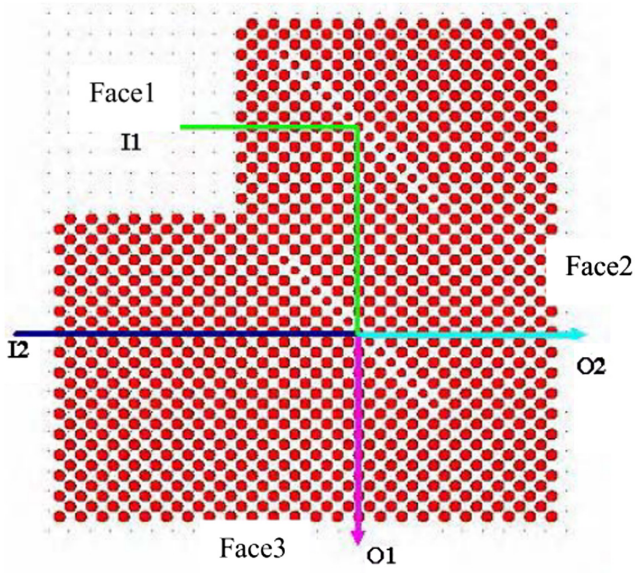

Fig. 6 Design of OR and XOR gates using 2D photonic crystal.

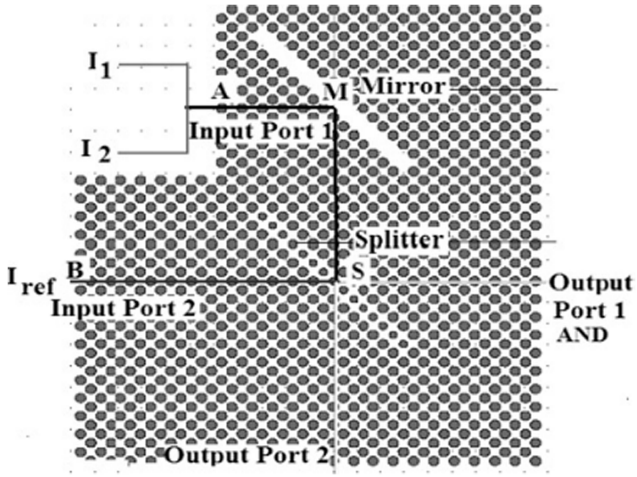

Fig. 7 Structure of AND gate.

The AND gate based on the self-collimated beam was proposed in Ref. 59 for the application of photonic-integrated structures. A square lattice 2D PhC structure with Si ($n = 3.46$) rods in an air background was used. The width in the X-direction and the length in the Z-direction were $23\sqrt{2}a$ and $25\sqrt{2}a$, respectively. The structure consisted of two line defects with the defect rod radius (r_d) of $0.274a$ ($a = 301$ nm), as shown in Fig. 7. When r_d was $0.274a$, the transmitted and reflected power was equally divided. In the case of r_d being greater than $0.274a$, the phase difference between the transmitted and reflected beams was $-\pi/2$; otherwise, it was $+\pi/2$. For the AND gate operation, $I_1 = I_2 = I_o$ and the reference signal $(I_{ref}) = 0.5\,I_o$ were applied at the input ports 1 and 2. Depending on the phase difference applied at different input ports, constructive or destructive interference occurred. Destructive interference represented output for the AND gate. When none of the input was given, $0.5\,I_o$ was divided equally between two output ports, i.e., $0.25\,I_o$. When both of the inputs were applied, the output at defect 1 was $2\,I_o$, which became $0.75\,I_o$ after passing through defect 2, where destructive interference occurred. The threshold value to differentiate between logic 1 and logic 0 was $0.24\,I_o$. The average area used for the proposed design of the AND gate was $25 \times 10\ \mu m^2$, and the overall response time was <2 ps.

From Table 1, it can be observed that different researchers proposed different structures for designing different gates. The highest number of gates was designed by Ref. 56, in which AND, NAND, XNOR, and XOR gates are realized. The structure used by all researchers is rods in air with Si rods in an air background. But in the case of CR, the structure designed by Christina and Kabilan[57] for NOT showed the best performance, i.e., 30 dB. Also, gates designed using a self-collimated beam suffer from many disadvantages, such as low CR, large area, high cost due to large area, and guidance of signal in only the vertical and horizontal direction.

The advantages of the nonband gates and all-optical logic gates are very simple design and less time taken for the simulation, while the disadvantages are low CR, requirement of phase shifters, acquired large area, high cost due to large area, and signals are only guided in horizontal and vertical directions.

2.2 *Bandgap-Based All-Optical Logic Gates*

In bandgap-based all-optical gates, the bandgap of the structure is used to find out the hidden frequency ranges, which are unable to pass through the structure. One of the hidden frequencies is able to propagate through the structure by introducing different types of defects. Bandgap-based gates are generally designed using MMI, nonlinear Kerr effect, and interference. In Ref. 60, MMI structure layout-based AND and NOR gates were proposed, as shown in Fig. 8(b), with A and B as input ports and O_1 and O_2 representing signals with fixed phase and amplitude, which act as reference signals. The principle on which MMI devices work is known as the self-imaging phenomenon. In this phenomenon, the small field at the input excites

Table 1 Comparison between different types of nonbandgap-based all-optical gates.

Reference	Lattice type	TE/TM	Gate	Area	Contrast ratio (dB)	Bit rate (Tbit/s)	Operating wavelength (λ)	Lattice constant (a)	Rod material	Background material
Ref. 54	Square (rods in air)	TE	OR, XOR	—	17	—	1/0.194 (a/λ)	—	Si	Air
Ref. 55	Square(air holes in Si)	Both	Waveguide for gates	—	—	—	1550 nm	420.05 nm	Air	Si
Ref. 56	Square (rods in Si)	TE	NOT, OR, AND, XOR	—	30	—	1550 nm	0.4185 nm	Air	Si
Ref. 57	Square (rods in air)	TE	AND, NAND, XNOR, NOR	—	6	—	1555.1 nm	302 nm	Si	Air
Ref. 58	Triangular (rods in air)	—	XOR, OR	—	—	—	1550 nm	365 nm	Si	Air
Ref. 59	Triangular (rods in air)	—	AND	$25 \times 10\ \mu m^2$	—	—	1.5 μm	0.45 μm	Si	Air

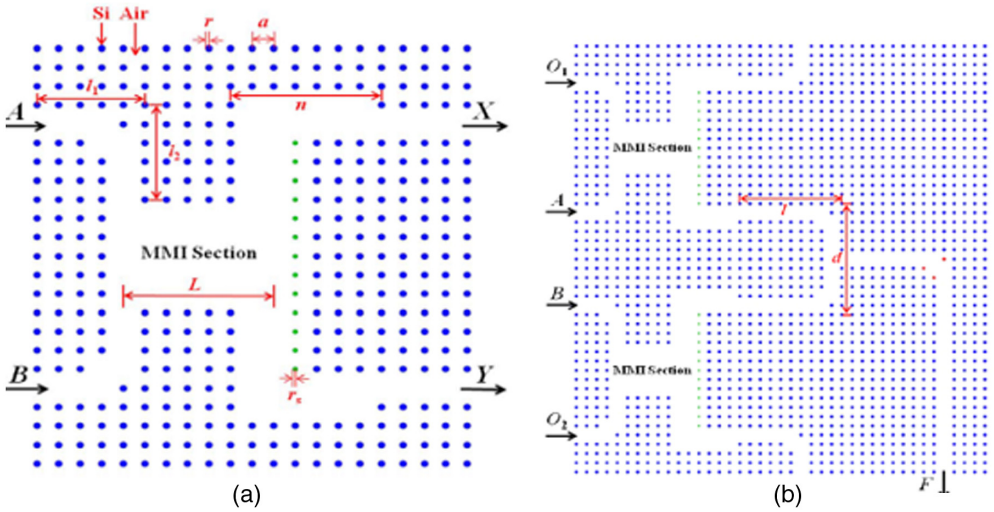

Fig. 8 (a) Structure of XOR/XNOR gates and (b) structure of AND and NOR gates.

guided modes in the effective area, which represented interference in that area. Binary phase shift keyed (BPSK) signals are used as input logic values because generally in MMI input values are represented by phase of the input signals whereas output logic value are represented by amplitude regardless of phase. In other words, with the proper generation of the input signal phase, either a signal was generated at the output, which was considered logic 1, or it was degenerated, which corresponded to logic 0, depending on how the different input phase signals interact in the MMI. The MMI structure behaves as a directional coupler to send the output to one of the output ports, which can be achieved by designing the MMI coupler with the proper selection of parameters for the effective area to obtain output from the specific port. In the proposed structure, Si material was used for the rods with air as background aligned in square lattice geometry. A and B were the input ports with X and Y as the output ports of the XOR/XNOR gate structure, as shown in Fig. 8(a). Logic "0" was expressed as signal input when there was phase shift of π at port A, while logic "1" was explicit with phase 0 whether at port B, logic "0" was expressed with a phase shift of $3\pi/2$ while logic "1" with phase $\pi/2$. For the realization of the AND gate proposed in Fig. 8(b), inputs A and B with phase π represented logic "0" while phase 0 represented logic "1." Logic "0" was set at O_1 and O_2 with a phase shift of $3\pi/2$. To design the NOR gate, the only difference was that O_1 and O_2 were locked at logic "1", represented by a phase shift of $\pi/2$. The CR achieved for the AND gate was 21 and for the NOR operation was 19 dB.

MMI-based AND and XOR logic gates were proposed in Ref. 61, as shown in Fig. 9, having A and B input ports of the device and X and Y output ports. It was built using the triangular lattice geometry with SiO_2 as the background material with Si rods. The structure has the lattice constant, rod radius r, while the rods at the bend had radius r_w, r_x, r_y, r_z, which were optimized so that there was maximum transmission at the output ports. The parameters chosen for the MMI region were a width W of $2\sqrt{3}a$ and a length L, where W_n means a waveguide, which was created by totally removing n lines of rods in PhC. To design the XOR gate, the length taken for the MMI was $9a$. An input signal was launched at port A with the phase shift of π, which expressed logic "0" while on port B, the signal was launched with a phase shift of $-\pi/2$, which expressed logic "1" and generates logic "1" at the output port. When there was a phase of π at port A, which expressed logic "0" and another signal with phase shift $\pi/2$ at port B expressed logic "0," there was a generation of logic "1" at the output. In another case, when a signal with a phase shift of π at the input port A expressed logic "0" while the signal with phase $\pi/2$ at port B expressed logic "0," there was logic "0" detected at the output. When both inputs at port A and port B represented logic "1" with the phase shift of 0 and $-\pi/2$, logic "0" was detected at the output port. Using the same structure, the AND gate was realized by changing the length of MMI to $10a$ and properly selecting input signal phases. A CR of about 6.79 dB was achieved for both AND and XOR logic gates.

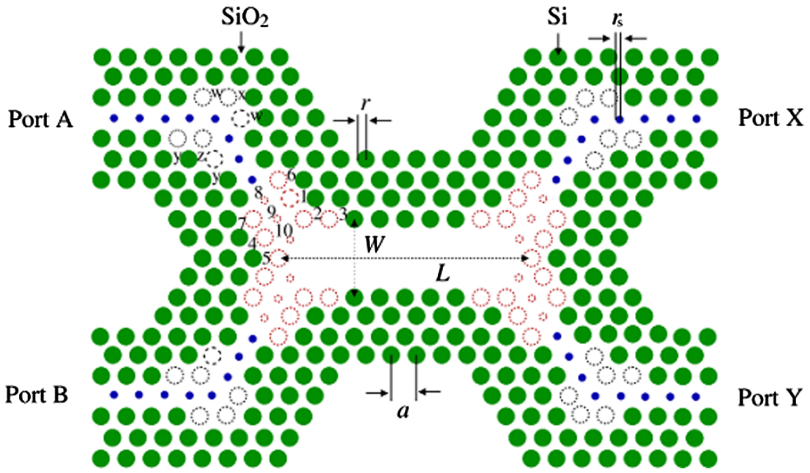

Fig. 9 Schematic of AND and XOR gates based on MMI.

In Ref. 62, another structure for XOR, NAND XNOR, and OR gates based on MMI was proposed, as shown in Fig. 10, with A and B as the input ports and C and D as the output ports. The structure was built on the triangular lattice geometry of PhC with Si rods with SiO_2 as the background material and having a lattice constant a and radius r. The radius of rod B is R; by shifting the distance of $d = 0.5a$, rod A was optimized with the MMI region of width W5 and length $L = 4a$. In the case of the XOR gate, logic "1" was expressed by input signal with phase 0 for port A while logic "0" was represented by a signal with a phase shift of π. For port B, the phase shift of $-\pi/2$ expressed logic "1" while the phase of $\pi/2$ expressed logic "0." All other gates were expressed with the different combinations of the phase of the input signals at port A and port B. The extinction ratio achieved for the XOR, XNOR, NAND, and OR gates was 28.6, 28.6, 25, and 26.6 dB, respectively, in the C-band.

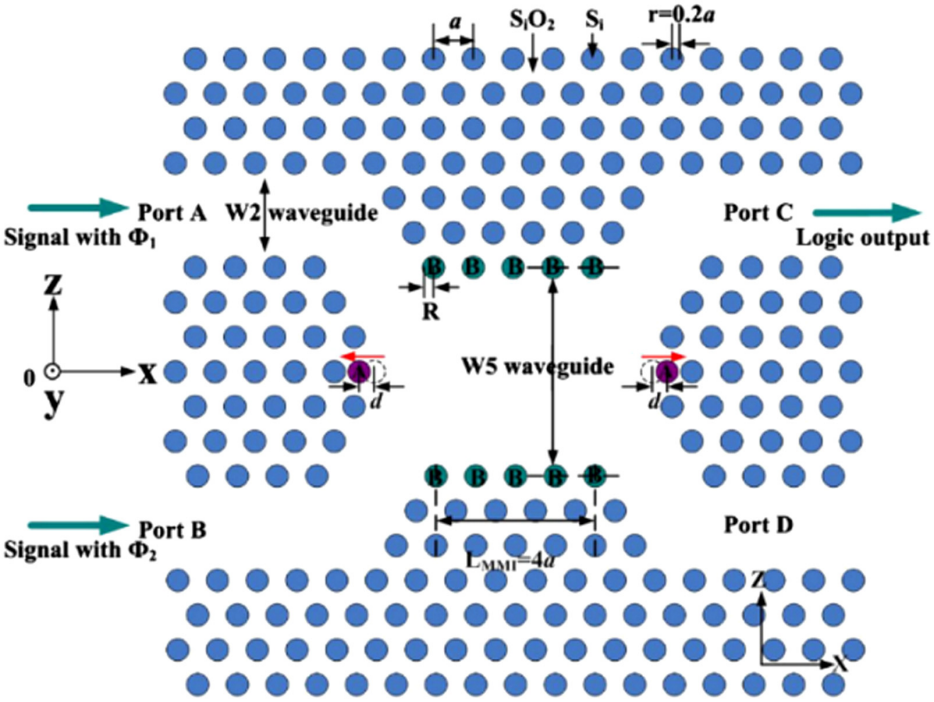

Fig. 10 Schematic structure of XOR, XNOR, NAND, and OR gates using triangular lattice geometry.

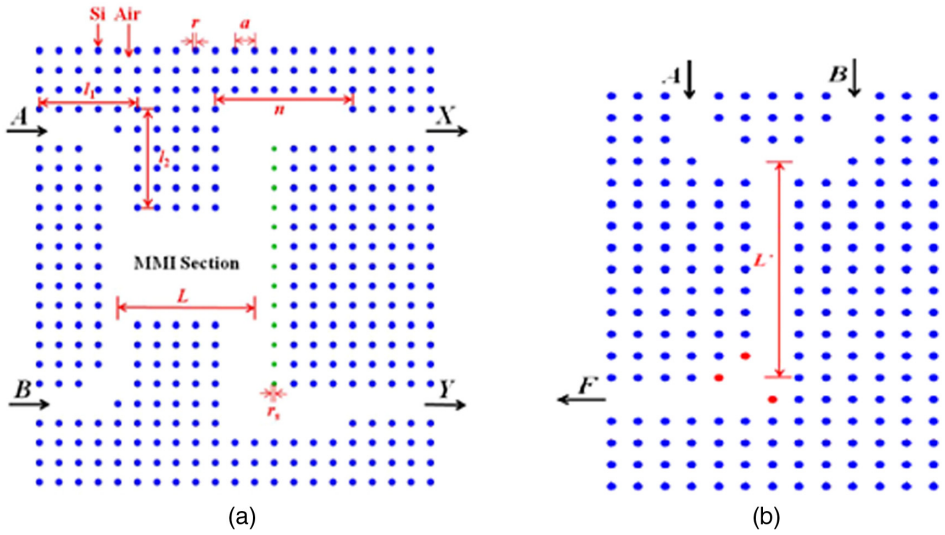

Fig. 11 (a) Schematic of XOR/XNOR using BPSK signals and (b) structure of AND gate with nonlinear Kerr material rods.

The XOR, XNOR, and AND gates were proposed in Ref. 60 using the concept of BPSK signals in MMI. The device was constructed using Si ($n = 3.4$) rods in an air background aligned in a square lattice. The radius selected for holes was $0.18a$, where a was the lattice constant with a value of 522 nm. The operating bandwidth of the structure ranged from 0.333 to 0.341 (a/λ), which represented the C-band. The design of the XOR/XNOR gate, as shown in Fig. 11(a), consisted of two inputs A and B and two outputs X and Y.

For designing the structure, lengths l_1, l_2, and L were varied and found to be $5a$, $5a$, and $7a$, respectively, to achieve maximum power at the output. On input port A, phase 0 represented logic 1 and phase π was logic 0. On another input port B, $\pi/2$ represented logic 1 while $3\pi/2$ represented logic 0. With this combination of phases, XOR and XNOR gates were realized. Another structure for the AND gate was also proposed; it consisted of an L-branch waveguide, as shown in Fig. 11(b). There were three Kerr nonlinear type rods with a dielectric constant of 7 and radius $0.18a$, as shown in red in Fig. 12(b). The structure consisted of two input ports A and B, and one output port F. L, i.e., the waveguide length where the interference occurs, was set to $10a$. In the case of the AND gate, the output of logic 1 was only required when both inputs showed constructive interference at the L-branch waveguide; otherwise, logic 0 was obtained. The CR achieved was 21 dB for the AND gate and 19 dB for the NOR gate operation.

In Ref. 63, a 2D PhC structure for the XNOR, XOR, OR, and NAND gates that was built on square lattice geometry having Si rods in an air background was proposed. The structure was composed of 11×15 cylindrical rods. For designing a waveguide, a total of five rows were deleted, called W5 waveguide. The structure contained two input ports A and B, and output port Y, as shown in Fig. 12, and the radius chosen was $0.2a$ ($a = 600$ nm). The coupling length of $6a$ was selected accordingly to achieve twofold images of the input. The input values were taken in the form of phases while the output was in the form of intensity. Depending on the phase applied, constructive or destructive interference occurred at the output. When the phase difference between the input signals was 0, a high-intensity signal was received at the output port Y due to a single fold of higher intensity. When the phase difference was π, two input signals never interfered with each other and were reflected back to the input port, producing a negligible amount of light at the output port. In another case, when the phase difference was $n\pi/2$, the light from the input port was superimposed and reached the same intensity at the output port Y. Using the different combinations of phases, XOR, OR, NAND, and XNOR gates were realized. The CR achieved was 40.41 dB for XNOR/XOR logic and 37.40 dB for OR/NAND logic at the wavelength of 1550 nm with the response time of <0.131 ps.

In Ref. 64, the AND gate structure based on nonlinear Kerr materials was proposed. Kerr materials have the property of changing the refractive index of material by changing the input

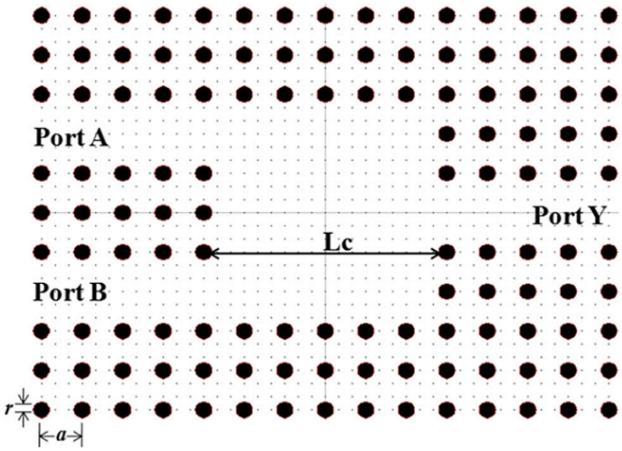

Fig. 12 Structure for XNOR, XOR, OR, and NAND gates based on multimode interference.

intensity. The refractive was calculated using the relation $n = n_0 + \Delta nI$, where I was the intensity, n_0 was the linear refractive index, and Δn represented the Kerr coefficient. With increasing or decreasing the intensity of the input signal, the refractive index changed, which changed many properties of the structure, such as operating frequencies, etc. The device consisted of two nonlinear ring resonators, as shown in Fig. 13, where the resonator acts as an add-drop resonator. Square lattice geometry of PhC was used to build the device with GaAs rods with a background material of borosilicate crown, which has a refractive index of 3.59 and 1.507. Nonlinear material used to build up the ring resonator was Si nanocrystals, which have a refractive index of 3.59 and Kerr coefficient of 10^{-16} m^2/W. Signals were polarized in the TM mode. The resonator made of linear material, as shown in Fig. 13, with the drop resonance wavelength of 1549.2 nm and input power of 33 $W/\mu m$ was required for nonlinear material, having a resonance wavelength of 1550.9 nm to act as the operating wavelength for the AND gate. As seen from Fig. 13, input ports were labeled A and B with port P being connected to the continuous signal. The signal from P coupled with the upper ring resonator when there was a signal at either A or B, which allowed no signal to go to the output port, which represented logic "0." When the signal was applied at port A, it coupled with the upper ring resonator and the signal P will not allow to couple with the upper resonator due to change come in the resonant frequency and signal P coupled with the lower ring resonator, which allows no signal at the output port. When there were signals at both input ports A and B, they coupled with the upper and lower resonators and signal P had no way to be coupled; hence, logic "1" was detected at the output port. The bit rate of the proposed logic gate was about 120 Gbits/s.

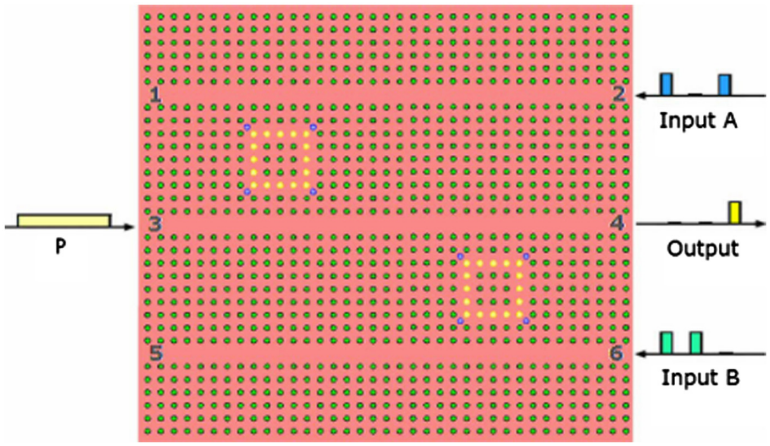

Fig. 13 Schematic of AND gate based on nonlinear Kerr material.

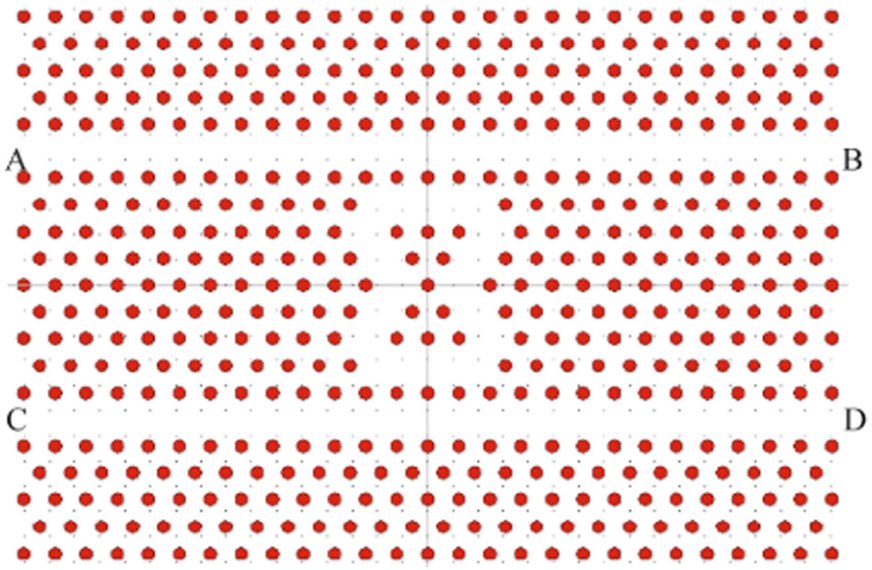

Fig. 14 Schematic of OR gate using nonlinear Kerr material.

Another structure for AND/OR/NOT gates based on nonlinear Kerr material was proposed by Pashamehr et al.[65] The structure has C and D as input ports while A was the reference port connected to the continuous signal and B was the output port, as shown in Fig. 14. The structure was made using the nonlinear Kerr materials with the ring resonator at the center, which resonates at a certain resonance frequency. When there was no input at port C or D, the signal from A coupled with the ring resonator and there was no output at port B, which represented logic "0." When there was input at either port C or D, they coupled the with the ring resonator and the resonance frequency changed, which lead the signal from A to propagate to port B, which represented logic "1."

In Ref. 66, a design for the NAND gate was proposed using the concept of nonlinearity in Kerr material with a PhC-based ring resonator, as shown in Fig. 15. In the proposed design, the ring resonator was designed using the 32×18 square array of chalcogenide glass rods ($n = 3.1$) in air. The radius of $0.2a$ was selected, where a was the lattice constant with a value of 640 nm. The PBG was calculated for the structure, and the wavelength of 1554 nm was found to be the resonant wavelength. After designing the ring resonator, it was seen that, with a power of 0.5 KW/μm^2 or greater, the refractive index of the material changed due to the Kerr effect, which changed the resonant wavelength of the ring resonator, as a result of which light cannot

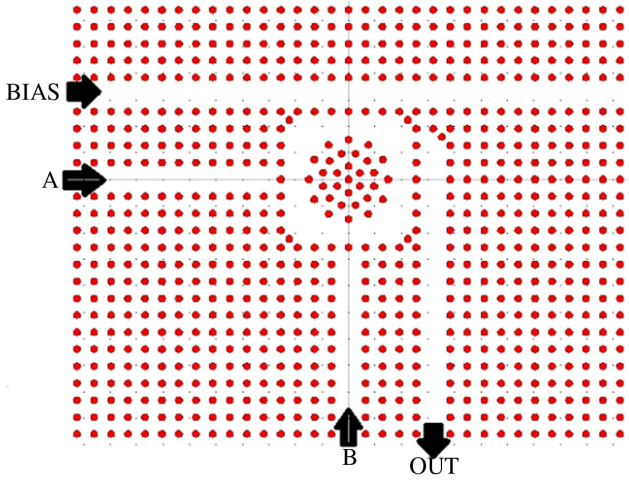

Fig. 15 Structure of NAND gate using nonlinear Kerr material.

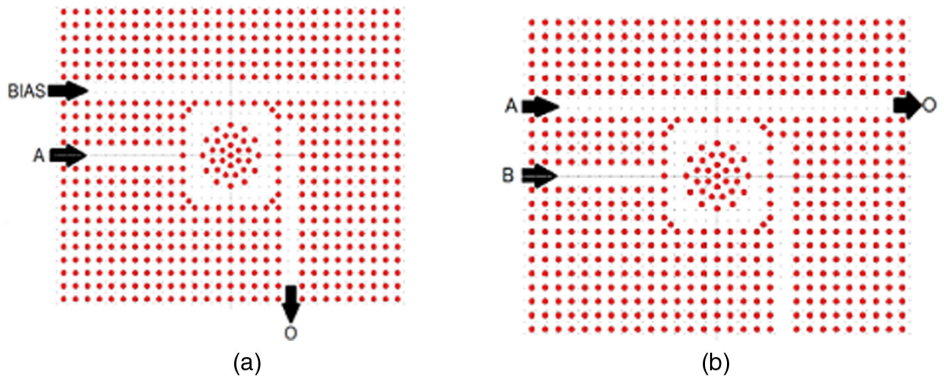

Fig. 16 (a) Layout of NOT gate and (b) layout of AND gate.

travel to the output port. After designing the ring resonator, the NAND gate structure was designed using 33×26 square lattices of dielectric rods. It consisted of three inputs A, B, and BIAS, and OUT was the output port, as shown in Fig. 15. When the input power of the ring resonator was <0.5 KW/μm^2, it resonated in the ring, and the output was generated at the OUT port; otherwise, there was no output, which verifies the logic of the NAND gate.

In Ref. 67, the structure of the NOT gate and the AND gate based on nonlinear Kerr material was proposed, as shown in Figs. 16(a) and 16(b). The structure has a ring resonator that connects to the waveguides for the input and output. A square lattice PhC geometry structure was used with rods of chalcogenide glass with an air background. The refractive index and Kerr coefficient of chalcogenide glass were 3.1 and 9^{-17} m^2/W with signals that were TM polarized. The drop resonance wavelength of the ring resonator was 1550 nm, which changed the power density to be higher than 1 KW/μm^2, which is the known threshold value. In the case of AND operations, as shown in Fig. 16(b), the operating wavelength of 1550 nm was required with 0.5 KW/μm^2 power density; when there was input at port A, only the signal after coupling with the resonator went to port O of Fig. 16(a), which represented the NOT gate and no signal was at the output O in Fig. 16(b). In the AND gate structure, when there was a signal at both input ports A and B, the input at B coupled with resonator while the input from port A propagated to port O, which represented the logic "1."

In Ref. 68, OR, NOR, XOR, NOT, NAND, AND, and XNOR gates were proposed on the principle of interference in the PhC, where A and B were the input ports and port R was the reference port, which was customized accordingly to perform as a specific gate, as shown in Fig. 17. Interference defects based all-optical logic gates depend on the type of defect introduced

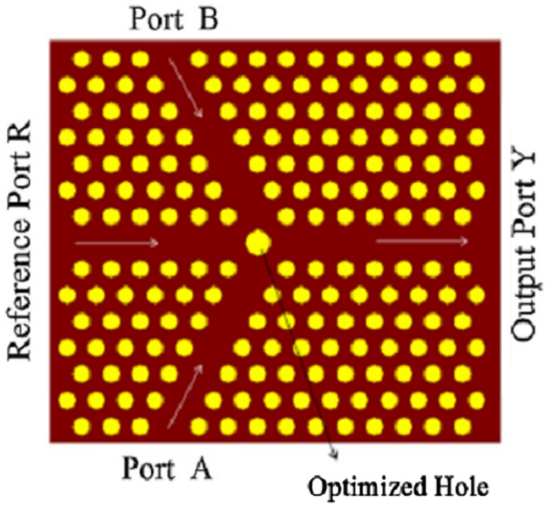

Fig. 17 Schematic of OR, AND, XOR, NOT, NAND, NOR, and XNOR gates.

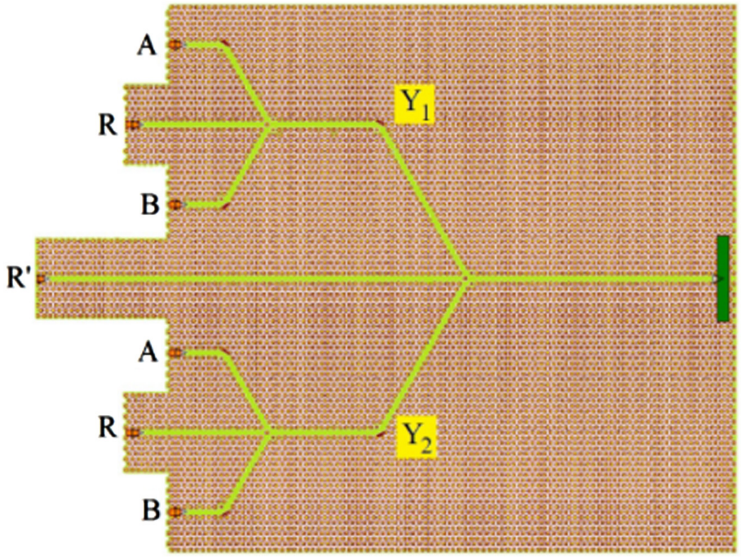

Fig. 18 Layout of AND gate built with NAND gate.

in the structure which relalizes the output of gate using the phenomenon of interference. The interference defect based all-optical logic gates are designed depending upon whether there is constructive or destructive interference occurs at the output by controlling the phase of the input signals. The constructive interference represented logic "1" while destructive interference represented logic "0." The structure was made on the triangular lattice PhC geometry with the Si rods with air as the background material. The waveguides were created by removing the holes, and the hole at the center was optimized to maximize transmission at the output port. The polarization of the operating signals was TE. For the realization of the AND gate, when there was no signal at either the A or B ports and the R signal was set to low, logic "0" was generated at the output port. Between A and B, if either signal was set to high with the reference signal set to high with a phase shift of π, then destructive interference was generated and logic "0" was observed at the output. If the signals for both inputs were set to high and the signal R was also set to high, then there was constructive interference and logic "1" was generated at the output port. The logic functions of XOR, NOR, NOT, OR, NAND, and XNOR were realized in the same way by varying the phase of the signal R for different combinations of the inputs.

In Ref. 69, a structure based on the interference-based effect with A and B as the input ports with R as reference port for realizing AND, XOR, OR, and XNOR gates was proposed, as shown in Fig. 18. Triangular lattice geometry of PhC was used to design the structure with air holes and Si as the background material. The input signals were TE polarized and all of the gates were realized using the proper combination of the NAND gates. Initial phases of the inputs A and B were set to 0 in all of the combinations with the signal R with phase π for realizing AND gate. The phase of R' was inverse of the signal R. Using the same concept of different combinations, other gates were realized using NAND gates.

In Ref. 70, a structure for the OR gate using the MZI was proposed. Si material was used for the rods with air as the background material, and it was built on triangular lattice geometry. The structure has the MZI at the center with upper and lower add-drop resonator connected to the two input arm and waveguides $\mathrm{Pin_A}$ and $\mathrm{Pin_B}$, as shown in Fig. 19. The operating signals were TE polarized. The two arms of the MZI have an equal length to achieve the constructive interference required to realize the OR gate. Between $\mathrm{Pin_A}$ and $\mathrm{Pin_B}$, if either of the input was launched, there was an output detected at the output port representing logic "1" and with the signal at both input ports; it interfered constructively due to having an equal length of MZI arms, which represented logic "1."

Another structure based on the interference effect was proposed by Ref. 71 for realizing OR, AND, XOR, and NOT gates having input ports named A and B with O as an output port. Square lattice geometry was used to design the structure with Si material for the rods and air as the

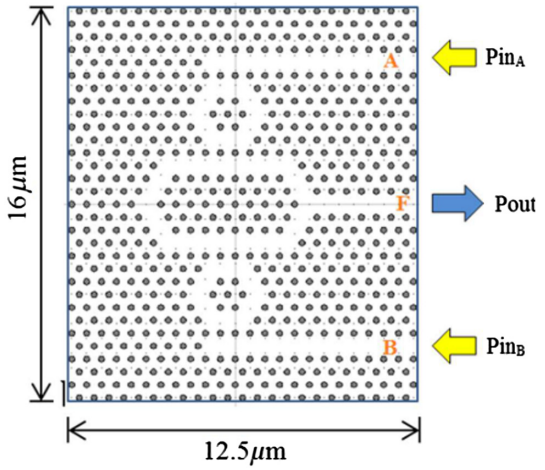

Fig. 19 Structure of OR gate with A and B as inputs.

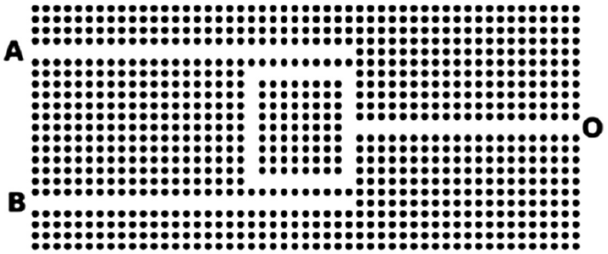

Fig. 20 Structure of OR gate with A and B as input ports.

background material. In Fig. 20, it is seen that there was a ring resonator and waveguides made by removing the rods, which were attached to the input as well as output. The input signals are TM polarized. When there was a signal at either A or B, there was a coupling between input signals in the resonator, where the coupled signal propagated in the clockwise direction (CW), whereas another part propagated in a counter-clockwise direction (CCW). Both the CW and the CCW interfered with each other constructively at the entry of the output waveguide, which represented logic "1"; when both signals were given due to symmetry, they interacted constructively, which gave logic "1" at the output. Similarly, by optimizing the size of the ring resonator, such as length and width, other gates were designed.

In Ref. 72, a structure for the realization of the NAND gate and different structures was proposed for realizing OR, AND, XOR, NOT, NOR, and XNOR gates. Square lattice geometry with germanium rods in an air black background was used to design the structure. For the realization of gates, all of the inputs and ref signals will be in the same phase. In Fig. 21, 1 represented the XOR gate while 2 represented the OR gate. The NAND gate was implemented using the unique combination of OR and XOR gates. One input of each XOR gate and a reference signal was set at logic "1" so that the output of every XOR gate was inverse of its input value. Two waveguides were formed to reach the output of the XOR gates to OR by maintaining the signals in phase. When there were no signals at input A or B, the ref signal produced logic "1" at the XOR output, which when reached the OR gate produced logic "1" as output. In another case, when there was input at A and B simultaneously, there was destructive interference, which lead to logic "1" as the output of one XOR gate while another gave logic "0" as the output, which when propagated through the OR gate gave logic "1."

Another structure for NAND and NOR gates based on the interference phenomenon was proposed by Ref. 73 with square lattice geometry of Si rods in an air background, as shown in Fig. 22. The NOT gate at the output was used to invert the output obtained from the AND/OR logic gate. It was because of the phase of the REF2 that the NOT gate inverted the logic.

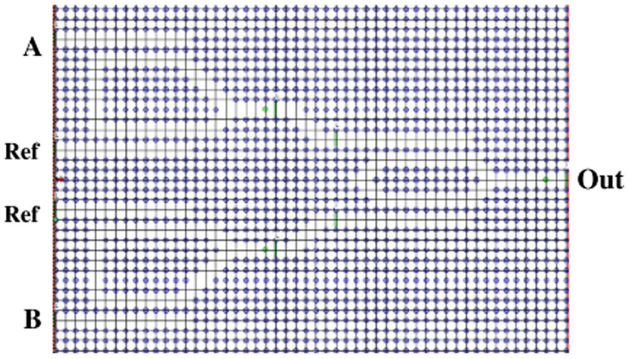

Fig. 21 Structure for NAND gate.

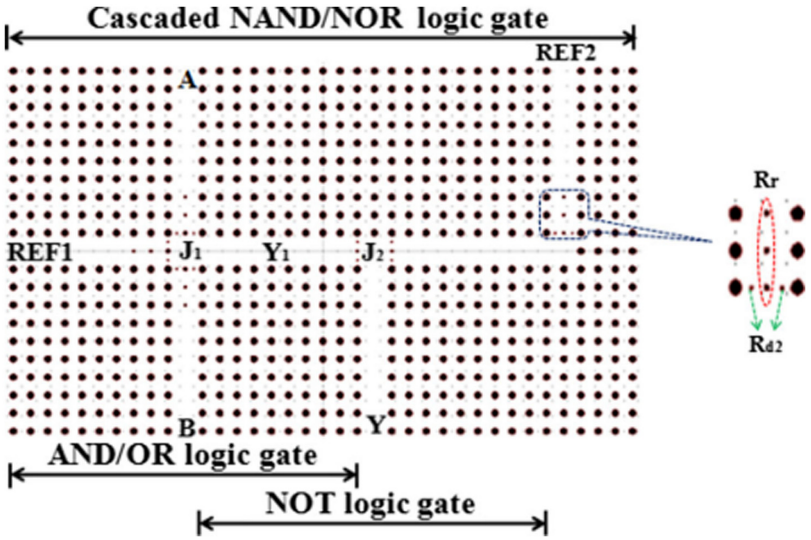

Fig. 22 Cascaded logic gate for NAND/NOR functions.

If the output of the AND/OR gate was logic "1," REF2 blocked it due to the destructive interference with the result of the AND/OR logic gate. If logic "0" was the output of the AND/OR logic gate, then there will be negligible power transfer due to destructive interference because the phase of REF1 had no affect while REF2 gave logic "1" at the output Y. Using these different combinations of the phases, all possibilities were realized.

In Ref. 74, interference defect-based OR, XOR, NOT, XNOR, and NAND gates were proposed. The structure was built using triangular lattice geometry with silicon cylindrical rods in the air. The lattice constant (a) and diameter were chosen as 875 and 495 nm, respectively. The distance between the inputs A and B was 10.5 μm. As seen from Fig. 23, it was a symmetric design. It was used to design gates, where constructive interference was required in case both inputs were logic 1, which was possible due to having the same defect length of both inputs. In the case of either A or B equal to logic 1, the light passed through the output port C, which realized the OR gate logic. In the case of the XOR gate, the line defect for input B was extended so that constructive interference did not occur and all other gates were realized by varying the length of line defect and introduction of reference signals. The highest CR of 20 dB was achieved in the proposed design.

In Ref. 75, two different designs for AND and OR logic gates were proposed. The parameters that remain the same in both designs were the refractive index, diameter, and lattice constant with the values of 3.59, 0.2 μm and 0.54, respectively. Both structures were arranged in a triangular lattice with circular rods of Si in the air background. As seen from Fig. 24(a) for the AND gate, it has two line defects, two ring cavities, and one Y-branch waveguide. A and B were inputs

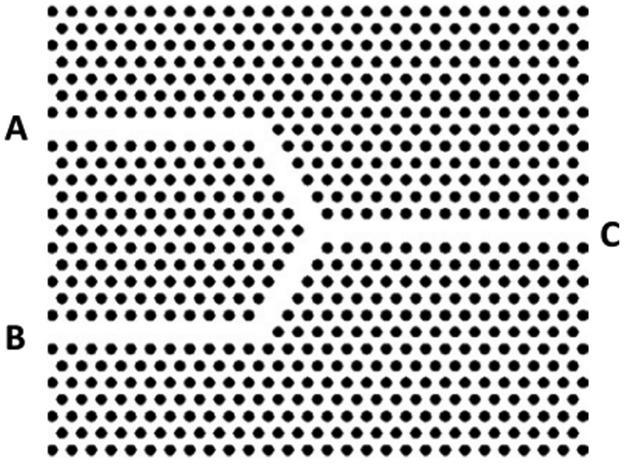

Fig. 23 Structure for OR gate in 2D photonic crystal platform.

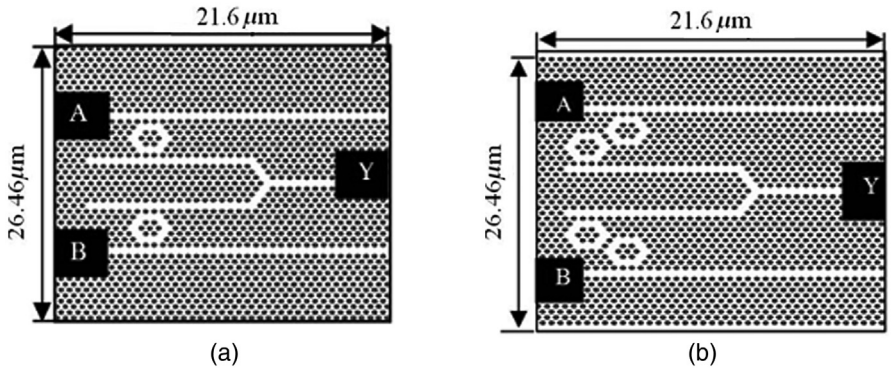

Fig. 24 (a) Structure for OR gate and (b) structure for AND gate.

while Y was the output. The input wavelength was set to 1.5 μm, which was the center wavelength of the ring cavities. If there was input at either of the ports or at both ports, the output was logic 1; otherwise, it was logic 0. In the AND gate, as shown in Fig. 24(b), there were two line defects, four ring cavities, and one Y-branch waveguide. There were two ring cavities added because they can drop the signal more and fewer signals will reach the output. The signal with intensity <0.5 was considered logic 0, which verified the logic of the AND gate, while the transmitted power of the OR gate was >0.5. Bit rates for the OR and AND gates reported were 0.5 and 0.208 Tb/s.

Another structure for NOT, NOR, XNOR, and NAND gates based on the interference phenomenon was proposed by Ref. 76. Si rods in the air were aligned in square lattice geometry. There were two different structures proposed, one for the NOT gate using one T-waveguide and the other for NOR, XNOR, and NAND gates using two T waveguides made by removing holes. A reference port with a phase shift of 180 deg was added to perform different logic operations. When the phase difference was $2k\pi$, there was constructive interference; otherwise, destructive interference occurred. There were small holes r_{j1}, r_{j2}, r_{j3} of impure flint glass ($n = 1.92$) material added to reduce back reflections. In the NOT gate structure, as shown in Fig. 25(a), when input A and the reference port input were in phase, logic 0 was detected, and in other cases, logic 1 was detected. In Fig. 25(b), the NAND, XNOR, and NOR gate structure was realized using different combinations of phases of input signals. The fastest response of the proposed structure was 0.35 ps. The size of the NOT gate was 5.04×5.04 μm^2, and the size was 8.04×5.04 μm^2 for the NAND, XNOR, and NOR gates.

In Ref. 77, a structure for the NOR and AND logic gates was proposed. The design was made on the triangular lattice geometry of Si rods in an air background with a lattice constant (a) of

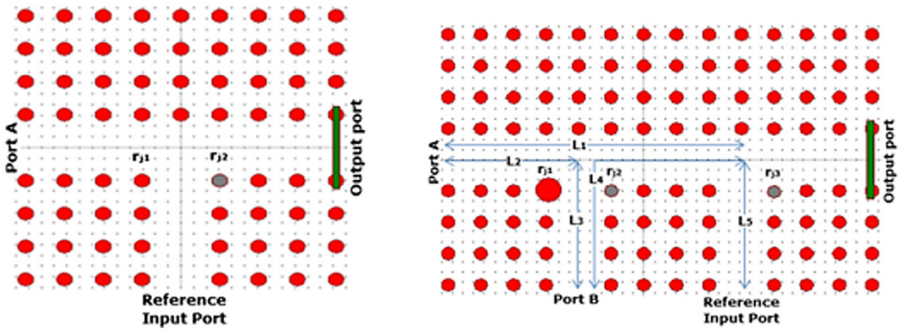

Fig. 25 (a) Structure for NOT gate and (b) structure for NAND, XNOR, and NOT gates.

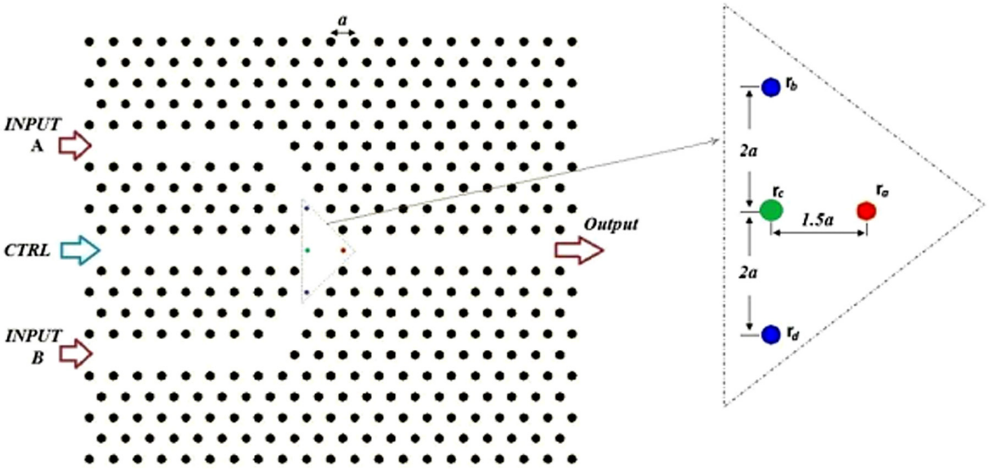

Fig. 26 Structure for NOR and AND gates.

580 nm and a rod radius of $0.2a$. The same structure was used for realizing both gates. As seen from Fig. 26, it has three inputs A, B, and CTRL and the output. The CTRL input was set active only in the case of the NOR gate. As seen from the structure, three rods with their radius set to $0.6r$ to reduce back reflections were not deleted. In the case of the XOR gate, if there was no input, the output was the CTRL signal, and in all other cases, there was no output due to destructive interference. In the case of the AND gate, a different combination of input phases was used to verify the AND gate logic. The bit rate achieved for the NOR and AND gates was 1.54 Tbits/s.

The structure in Fig. 27 was proposed by Ref. 78 to realize all-optical AND/OR gates. The structure had square lattice geometry with the Si rods in the air background. It consisted of one ring resonator, which was optimized by varying the rod radius so that that it resonated at the resonance frequency, and four waveguides were made by removing the rods, which are connected to input ports A and B, and outputs 1 and 2. It had an inner ring radius of $0.15a$ while another rod radius was $0.2a$, where a was the lattice constant. When there was input at port A and no input at port B, the input from A that coupled from the resonator in the clockwise direction at the output occurred at the output1, which realized the AND output as logic "0", and output 2, which realized the OR gate output as logic "1." When there was no input at either input port, there was no output at either output port. When $A = 0$ and $B = 1$, the input from B coupled with the ring resonator and having logic "1" at the output 2 realized the OR gate while the output at port 1 was logic "0" for the AND gate. When there were inputs at both inputs, there was constructive interference, which lead to logic "1" at both outputs.

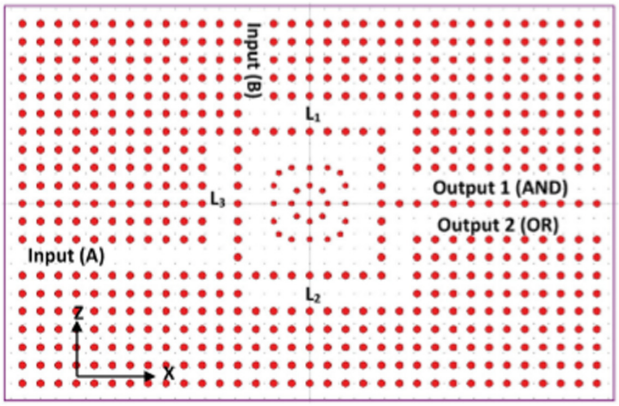

Fig. 27 Schematic of AND/OR logic gates.

Another structure for designing NAND, NOR, and XNOR logic gates based on the interference phenomenon in the PhC was proposed by Sankar Rao et al.[79] By only changing the phase of input signals, different logic gates were realized. Square lattice geometry with Si rods ($r = 0.2a$ with a of 0.6 μm) in the air was used to design structure, as shown in Fig. 28. It consisted of two input ports A and B with reference port R, and different gates were realized. There were certain modifications done in particular rods in structure to obtain the required output, i.e., $r_{j4} = 0.666$ μm, $r_{j1} = 0.24$ μm, $r_{j2} = 0.24$ μm, and $r_{j3} = 0.054$ μm. Also, there were some reflecting rods with different radii introduced for the reflection operation, i.e., $r_1 = 0.12$ μm and $r_2 = 0.084$, to achieve the desired output in the proposed structure. For designing the NAND gate, logic 1 was represented with a phase shift of 0 deg in the combination of inputs "10" and "01," while in the case of "'11," it was represented by a phase shift of 0 and 180 deg. The reference signal was set to 180 deg in "01" to achieve constructive interference, while in the case of "'11," phase was set to 180 deg to achieve destructive interference. The structure was the same for XOR and XNOR logic gates. The only difference was that by varying phase shifts between inputs, these gates were realized. The operating wavelength of the structure was 1550 nm. The CR achieved for NAND, NOR, and XNOR logic gates was 17.59, 14.3, and 10.52 dB, respectively. The structure had a size of 7.2×5.4 μm^2.

In Table 2, comparative analysis of bandgap-based all-optical logic gates is discussed on the performance parameters such as the CR and bit rate. The structure proposed by Parandin and Karkhanehchi[77] for AND and OR gates shows the highest CR of 17.95 dB and provides a bit rate of 6.76 Tbit/s. Bandgap-based gates based on the interference phenomenon provide a high CR and simpler design as compared to that of the other phenomena.

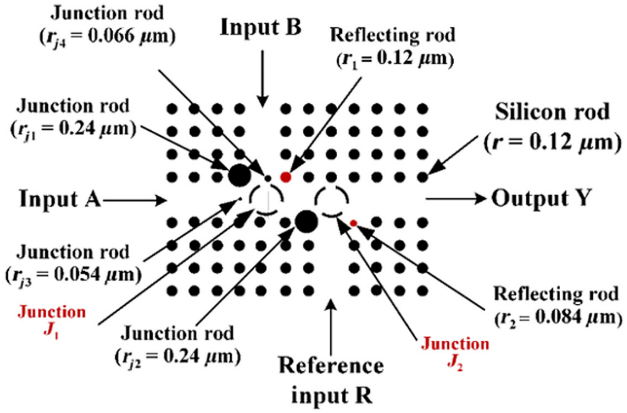

Fig. 28 Schematic of AND/OR logic gates.

Table 2 Comparison between different types of bandgap-based all-optical logic gates.

Reference	Lattice type	TE/TM	Gate	Area	Contrast ratio (dB)	Bit rate	Operating wavelength (λ)	Lattice constant (a)	Rod material	Background material
Ref. 60	Square (rods in air)	TM	XOR, XNOR, AND, NOR	—	AND-39 NOR-47	—	1530–1565 nm	522 nm	Si	Air
Ref. 61	Triangular (rods in SiO_2)	—	XOR, AND	$9.9 \times 10.8\ \mu m^2$	XOR-13.3 AND-6.79	—	1550 nm	0.45 nm	Si	SiO_2
Ref. 62	Triangular (rods in SiO_2)	TM	XOR, XNOR, NAND, OR	$6.9 \times 6.7\ \mu m^2$	XOR-28.6 XNOR-28.6 NAND-25 OR-26.6	—	1530–1565 nm	430 nm	Si	SiO_2
Ref. 63	Square (rods in air)	TE	XNOR, XOR, OR, NAND	6.4×8.8 m	37.4–40.41	7.67 Tb/s	1550 nm	600 nm	Si	Air
Ref. 64	Square (rods in borosilicate crown)	TM	AND	—	6.93	0.12 Tb/s	1550.9 nm	455 nm	GaAs	Borosilicate
Ref. 65	Triangular (rods in air)	TM	AND, OR, NOT	—	—	—	1550 nm	616 nm	Chalcogenide glass	Air
Ref. 66	Square (rods in air)	TM	NAND	—	—	—	1554 nm	640 nm	Chalcogenide glass	Air
Ref. 67	Square (rods in air)	TM	NOT, AND, NAND	—	—	—	1550 nm	630 nm	Chalcogenide glass	Air
Ref. 68	Triangular (holes in Si)	TE	AND, OR, XOR, NOT, NAND, NOR	—	AND-8.76 XOR-8.49 NOT-5.42 NAND-9.59 NOR-5.42 XNOR-5.42	0.976 Tb/s	1550 nm	0.352 μm	Air	Si
Ref. 69	Triangular (holes in Si)	TE	NOT, AND, OR, XOR, XNOR, NAND	—	NOT-3.74 AND-11.47 OR-12.48 XOR-6.50 XNOR-6.50	0.461 Tb/s	1550	0.352 μm	Air	Si

Table 2 (*Continued*).

Reference	Lattice type	TE/TM	Gate	Area	Contrast ratio (dB)	Bit rate	Operating wavelength (λ)	Lattice constant (a)	Rod material	Background material
Ref. 70	Triangular (rods in air)	TE	OR	$12.5 \times 16\,\mu m^2$	7.27	0.8 Tb/s	1287.8 nm	—	Si	Air
Ref. 71	Square (rods in air)	TM	OR, AND, XOR, NOT	—	35	—	1354–1706 nm	0.65 μm	Si	Air
Ref. 72	Square (Ge in air)	TE	OR, AND, XOR, NOT, NOR, NAND, XNOR	AND-$10.6 \times 11.6\,\mu m^2$ NAND-$28.4 \times 19.8\,\mu m^2$	AND-6.02 XOR, NOT-12.155 NOR-9.02 NAND-8.58	NAND-3.8 Tb/s, XNOR-77.6 Tb/s, XNOR-9.59 Tb/s	1550	0.58 μm	Ge	Air
Ref. 73	Square (rods in air)	TE	AND, NOT, OR, NAND, NOR	AND/OR-$12.24 \times 12.24\,\mu m^2$ NOT-$8.64 \times 12.24\,\mu m^2$	AND-11.74 OR-9.99 NOT-54.52 NAND-10.57 NOR-8.60	6.67 Tb/s	1550 nm	0.6 μm	Si	Air
Ref. 74	Triangular (rods in air)	TM	OR, XOR, NOT, NAND, XNOR	24.5×23.6 35×30.6	20	—	1550	875 nm	Si	Air
Ref. 75	Triangular (rods in air)	TM	OR, AND	21.6×26.46	6	AND-0.208 Tb/s OR-0.5 Tb/s	OR-1529 nm AND-1538	0.54 μm	Si	Air
Ref. 76	Square (rods in air)	TE	NAND, NOR, NOT, XNOR	NOT-$5.04 \times 5.04\,\mu m^2$ NOR/XNOR/ NAND-8.04×5.04	NOT- 8.59 NOR-4.94 XNOR-6.71 NAND-7.45	—	1430–2120	600 nm	Si	Air
Ref. 77	Triangular (rods in air)	TE	NOR, AND	—	—	1.54 Tb/s	1550 nm	580 nm	Si	Air
Ref. 78	Square (rods in air)	TE	AND, OR	$19.8 \times 12.6\,\mu m^2$	9.74–17.95	AND 6.76 Tb/s OR-4.74 Tb/s	1.52 μm	0.6 μm	Si	Air
Ref. 79	Square (rods in air)	TE	NAND, NOR, XNOR	7.2×5.4 μm	17.59, 14.3, 10.52	—	1.55 μm	0.6 μm	Si	Air

3 Conclusion

Due to the increasing demand for high speed and bandwidth, it is difficult to think of designing the optical computers without designing basic building blocks, i.e., all-optical logic gates. In this review, a detailed overview of different PhC-based techniques used to build all-optical logic gates is discussed and comparison is done based on different parameters, such as the CR, bit rate, and any area with many more parameters.

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