

PROCEEDINGS OF SPIE

Alternative Lithographic Technologies VII

Douglas J. Resnick
Christopher Bencher
Editors

23–26 February 2015
San Jose, California, United States

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Published by
SPIE

Volume 9423

Proceedings of SPIE 0277-786X, V. 9423

SPIE is an international society advancing an interdisciplinary approach to the science and application of light.

Alternative Lithographic Technologies VII, edited by Douglas J. Resnick, Christopher Bencher,
Proc. of SPIE Vol. 9423, 942301 · © 2015 SPIE · CCC code: 0277-786X/15/\$18
doi: 10.1117/12.2192291

Proc. of SPIE Vol. 9423 942301-1

The papers included in this volume were part of the technical conference cited on the cover and title page. Papers were selected and subject to review by the editors and conference program committee. Some conference presentations may not be available for publication. The papers published in these proceedings reflect the work and thoughts of the authors and are published herein as submitted. The publisher is not responsible for the validity of the information or for any outcomes resulting from reliance thereon.

Please use the following format to cite material from this book:

Author(s), "Title of Paper," in *Alternative Lithographic Technologies VII*, edited by Douglas J. Resnick, Christopher Bencher, Proceedings of SPIE Vol. 9423 (SPIE, Bellingham, WA, 2015) Article CID Number.

ISSN: 0277-786X

ISBN: 9781628415254

Published by

SPIE

P.O. Box 10, Bellingham, Washington 98227-0010 USA

Telephone +1 360 676 3290 (Pacific Time) · Fax +1 360 647 1445

SPIE.org

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Printed in the United States of America.

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Introduction

The semiconductor industry has relentlessly marched down a path which has enabled device dimensions with half pitches as small as 15nm to be realized. Spacer multiple patterning in particular has been invaluable for the NAND Flash market and, in recent years, has found its way into both DRAM and logic based devices. Spacer patterning has not only introduced additional processing costs, but also enabled scaling greater than the tradition 0.7 factor, with multiple device makers continuing to report lower cost per function.

Several options exist to extend the semiconductor technology roadmap beyond the 14nm node. Both top down and bottom up lithographic technologies are now part of the ITRS roadmap, and among the candidates are maskless lithography, nanoimprint lithography and directed self-assembly (DSA). In addition to enabling cost effective solutions for the logic and memory markets, these lithographic solutions also hold the promise of enabling many other key markets that also require high resolution lithography. Included in this list are patterned media for hard disk drives, high brightness light emitting diodes and several display related applications.

Any lithographic technology needs to address several key requirements beyond just resolution. Critical parameters include layout restrictions, defectivity, overlay, grid correction, throughput and cost. In addition, any consideration for high volume manufacturing must include a supporting infrastructure which allows a seamless integration of the new technology into a production facility. The goal of the Alternative Lithography Conference was to review new lithographic solutions, as well as monitor the progress of technologies that could one day become mainstream. The conference did not limit itself to the options listed in the ITRS roadmap and also considered innovative approaches including: plasmonics, micromirror optical lithography, interferometric lithography, tip-based nanolithography, scanning array lithography, dip pen printing and drop-on-demand inkjet lithography.

This year's conference consisted of more than 78 invited and contributed presentations on these topics. The conference was held over three and a half days, with fourteen oral sessions, a poster session and a panel discussion.

The Alternative Lithography Conference was highlighted by three Keynote presentations Monday afternoon. Speakers included: Dr. Yan Borodovsky from Intel, Dr. Toshiaki Ikoma from Canon, and Dr. Dan Millward of Micron. Dr. Borodovsky emphasized the need for edge placement on complimentary patterning layers and suggested that work was needed on selective growth mechanisms to meet pattern placement specifications. Dr. Ikoma introduced Canon's nanoimprint lithography program and discussed both progress in the technology space, as well as introducing new imprint systems to the community. Dr. Millward gave an insightful overview on DSA and discussed both progress

made, technical hurdles and benchmarked performance versus SAQP (spacer quadruple patterning).

DSA still commands the most attention at this conference and speakers from Intel, TEL and elsewhere reported significant improvements on defect density, for both hole and dense line patterns.

Step and repeat nanoimprint lithography was covered by speakers from Toshiba, Canon, Canon Nanotechnologies and Dai Nippon Imprinting. The invited talk from Toshiba reviewed both the progress made, as well as infrastructure areas where help was still required.

Beam lithography talks were highlighted by two presentations: One from IMS Nanofabrication, which reviewed their progress on a multi-beam mask writer; and a second from Sematech and Zeiss, which discussed the progress made on a multibeam inspection tool for both wafers and masks.

A conference of this magnitude cannot be successful without a dedicated program committee, and our thanks go out to all the committee members for their tireless review of abstracts and help with the organization of the individual sessions. Special thanks are also due to Alex Liddle and Martha Sanchez for hosting a panel discussion on the topic: Dimensional Scaling, Design Optimization, and Metrology: What are We Missing?

Next year, Chris Bencher from Applied Materials and Joy Cheng from IBM will chair the conference. We look forward to your continued support through the submission of abstracts and manuscripts, and look forward to seeing everyone next year.

Douglas J. Resnick
Christopher Bencher