Patterning Challenges in the sub-10 nm Era

Moshe E Preil
GLOBALFOUNDRIES, 2600 Great America Way, Santa Clara, CA 95054

ABSTRACT

Historically, progress in lithography has been driven by steady advances in exposure tool and optical technology; shorter wavelength, higher numerical aperture (NA) and resolution enhancement techniques to drive the k_1 factor as close as possible to the physical limit. Over the past decade, however, the pace of progress has been gated more by patterning – what we do after the resist image is printed – than by higher resolution imaging. The emphasis on patterning rather than just printing has created new pressures in many parts of the overall process, beginning with the design itself. The breakdown of lithographic error budgets into CD and OL tolerances has given way to total edge placement error (EPE) budgets where CD, OL and edge roughness, as well as film and etch variations, must all be controlled to meet the required tolerances. Contact hole and cut mask placement have likewise been tightened to single digit EPE budgets. Collaborative research between technology specialists in multiple areas, such as metrology, etch, process control and simulation, will all be required to deliver these patterning solutions for some years to come. This paper will describe some of these challenges in more detail, and suggest directions for future research to keep optical lithography relevant even below the 10 nm node.

Keywords: Patterning, metrology, process control, edge placement error

1. INTRODUCTION: HISTORICAL CONTEXT

One of the key goals of the invited talks which open these conferences is to establish a sense of what we should look forward to hearing and discussing in this forum within the context of the past history of this event. This year marks the 41st year that this conference is being held. The title is Optical Microlithography XXIX (29) because the name and numbering sequence have been reset several times, but the emphasis on optical lithography for semiconductor manufacturing has remained constant. Over the years this meeting has grown from a single conference to a symposium with seven related conferences. Topical conferences on metrology and process control, patterning materials, alternative lithography, EUV, design technology co-optimization and etch have branched out and in some cases eve outgrown the parent conference. Through all of these changes, this particular conference has endured and, to many of us, remains the central core of the symposium, as attested to by the number of joint sessions with other conferences.

Fig. 1 shows a sampling of papers given at this conference over the years[1]. The number peaked some years ago and has declined somewhat, but the conference remains strong with new topics gaining increased attention as others have split off into their own conferences. We note peaks in computational lithography in the early 90s, in DTCO in 2011, and especially in tools and applications around 2006 when immersion lithography assumed its current dominant role in leading edge lithography. Throughout this history, papers on exposure tools have retained a special place of interest here even as EUV tool papers moved off to a separate and larger conference.

The first decade of this conference saw steady evolutionary progress in exposure tools, with periodic revolutionary changes in technology. 1x scanners were replaced by 5x steppers and then to 4x step and scan tools; exposure wavelengths changed from g-line and i-line to excimer lasers, culminating in today's 193 nm ArF tools. Numerical apertures increased steadily from ~0.30 to 1.35 NA immersion tools[2]. However, as shown in Fig. 2, there has been no change in wavelength or NA in production for close to ten years, with EUV still serving a strong development role at least for a few more years.

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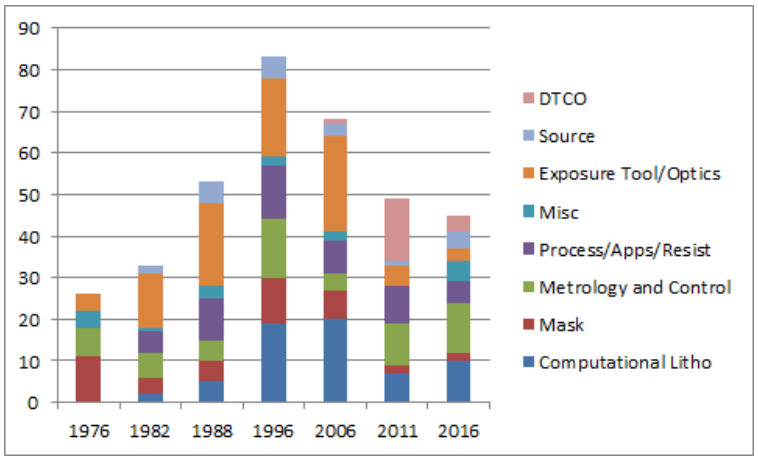

Figure 1: Oral papers by topic in selected years from 1976 to the present. The selection of which years to study is somewhat arbitrary, and binning of papers into specific categories is a highly subjective process. Note that the nature of the papers in each category has changed over the years.

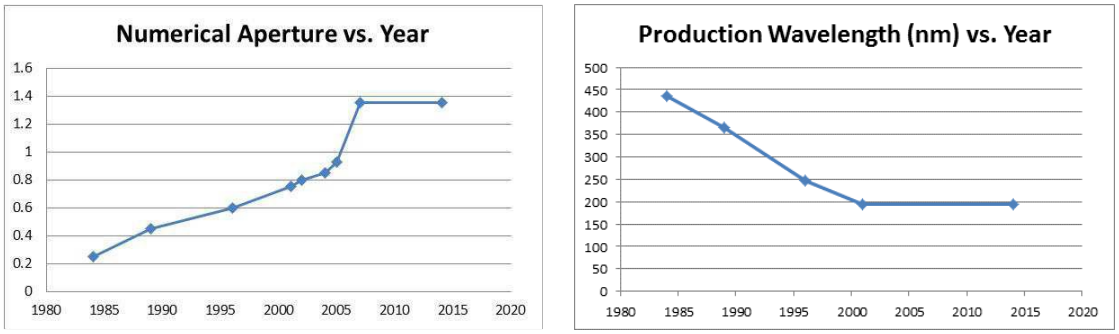

Figure 2: Numerical Aperture (left) and Production Wavelength (right) vs. year of introduction for leading edge exposure tools. Data represents an aggregate among multiple suppliers and users.

The tool manufacturers have certainly not been standing still. Each year new tools come to market with better performance. Productivity, overlay and focus control, increasingly complex illumination and lens corrections to manipulate the source distribution[3,4] and even the wavefront[5], have all made today's 1.35 NA tools more capable than their predecessors. But the basic fact remains; there has been no major advance in increasing resolution for close to a decade, even as we have moved from the 45-65 nm era to today's 14 nm production node, and even 10 and 7 nm nodes are being actively developed with the same core exposure technology.

These shrinks, as we all recognize, have been enabled not by printing much smaller features in resist, but by changing what we do with the resist after it is printed. The major advance has been the move to multiple patterning, either multiple exposure (LE^n) or sidewall spacer patterning such as self-aligned double or even quadruple patterning (SADP/SAQP). In many leading edge processes, the minimum feature size is not even determined by the resist pattern. The resist defines the starting pitch and the location where the pattern will be placed, but the actual critical dimensions and final pitch may be determined by films deposition and etch steps.

2. IMPACT ON DESIGN STYLES AND ARCHITECTURE

Another notable trend has been the emergence of "Design-Technology Co-Optimization" (DTCO)[6,7]. In contrast to the early days of lithography when almost any pattern was acceptable as long as it did not vary a very limited number of specific design rules, today's approach is to optimize the printability of a selected number of basic patterns to the exclusion of most others. Design rules have evolved from a few simple "do not do this" statements (typically establishing minimum line space dimensions and required overlap with other layers) to thousands of lines of complex code. The operating philosophy has migrated from "do anything that is not explicitly forbidden" to "try to design with only this limited set of pitches and dimensions". The process is highly iterative and requires intensive collaboration

between designers and lithographers. In fact, many lithography engineers today live as much in the world of layout and design as they do in the more traditional lithography world of computation, processes and tools.

This trend is summarized in Fig. 3, where we see the evolution of gate mask patterns from 2-dimensional designs to unidirectional gates over 2D active areas, and finally to unidirectional gate and active at a fixed pitch and CD. The impact on electrical design has not been trivial. Drive current is now quantized rather than continuously selectable, especially given the advent of FinFETs, and threshold voltage adjustment, formerly achieved by varying CDs, is now better done by tailoring implant and stress profiles using different work function materials.

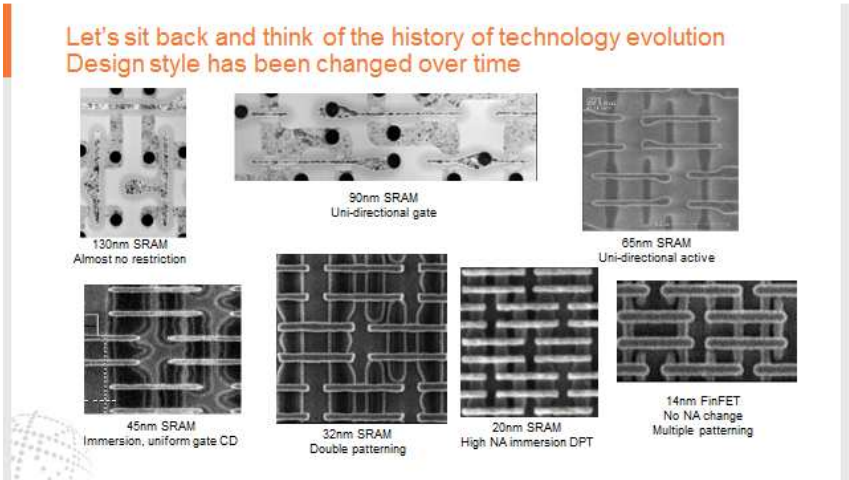

Figure 3: Technology evolution of gate and active design style over time (from Jongwook Kye, Semicon Korea 2016) [8]

As we approach the 7 nm node, one of the last holdouts for 2-dimensional design is likely to fall as well. Metal 1 patterning has remained bi-directional to avoid excessive penalties in terms of logic and memory cell sizes, as well as to minimize the number of layers that still require manual layout expertise and to reduce die cost. Although EUV has been demonstrated to be capable of patterning 2D metal 1 down to 7 nm node tolerances[9], it is still questionable if EUV can be commercially viable for production in time. The need for an optical backup solution is a strong driver for unidirectional metal 1, even at the expense of an additional local interconnect metal layer, in order to develop a single, wavelength agnostic design style.

The evolution of 1D patterns based on regular gratings makes printing the actual grating easier. At the same time, the key challenge has migrated to patterning the cut masks[10]. Removing or cutting a single line places great stress on the CD and overlay control required from the cut mask process. A 193i tool which requires some form of multiple patterning to pattern a grating pitch < 40 nm would face a daunting challenge trying to cut a line barely 20 nm wide at a specific location. Even if the tool could print such a tiny cut, the margin for CD and overlay tolerances, as well as line edge roughness, become increasingly difficult as the pattern shrinks. For a line/space pitch near 30 nm, the ability to excise a single line from a sea of lines is beyond the capacity of existing tools printing a single cut layer without some novel form of self-aligned cut process.

As the requirements for cut masks become a key limitation, the traditional breakdown of error budgets into distinct CD and overlay budgets becomes blurred. A new error budget is required combing CD, edge roughness, and overlay contributions from multiple layers to determine if the edge of the cut mask properly intersects the edge of the feature to be cut. Leading edge work to develop combined Edge Placement Error (EPE) budgets has become an emerging theme[11]. When multiple patterning is included, the EPE budget becomes a critical and complex study incorporating films and etch variations as well as lithographic parameters.

Cut mask engineering has attracted interest in several new technologies, none of which has yet reached production. Small, precise placed cuts would seem to be an ideal application of E-beam direct write (EBDW) since the major weakness of these tools – slow patterning speed – could be substantially relieved by only having to cover a limited

percentage of the die area[12]. Directed self-assembly (DSA) has also shown promise in being able to place tiny cuts within a larger, lithographically accessible template, and even producing 2 or 3 distinct cuts in a single guide pattern[13,14]. Other forms of hole shrinking processes have also been proposed[15], and EUV also has some distinct advantages in printing cuts instead of line/space patterns. All of these approaches must consider the full EPE budget to determine if the cuts can be placed where they are needed – and only where they are needed – to within the required tolerance.

3. FROM LITHOGRAPHY TO PATTERNING SOLUTIONS

A trend which has had a strong positive impact over the past decade has been the combination of simulation, metrology and process tool information to optimize and control lithography processes. The advent of computational lithography[16] and the ability to simulate full chip patterning performance[17] has enabled the maturation of optical proximity correction (OPC) from rule based to model based and finally to image based correction. At the same time, uniquely flexible illumination systems which can create freeform intensity distributions in the pupil plane enabled illumination profiles to be optimized for a specific set of target patterns. The era of source-mask optimization[18,19] (SMO) has allowed exposure tools to be pushed almost to the absolute physical limits of resolution. Even more complex approaches tailoring the phase of the wavefront as well as the intensity have been introduced, and computational solutions to predict and correct for the effects of lens heating based on full reticle layout data are now available[20,21]. In addition, full chip simulation including detailed lens and illumination models have been developed to improve pattern matching across scanner fleets[22,23].

Computational power and accuracy has also been utilized to improve metrology and inspection strategies. Full chip simulation based on design data and often augmented by reticle metrology and inspection data can identify potential lithographic "hot spots" where the process window will be the most limited and at risk of excursions[24]. Coupling this data to fab tools allows the automated creation of sampling and inspection plans targeted at the weak points. The advantages of such smart sampling have been applied successfully to both reticle and wafer inspection as well as to wafer level metrology[25,26].

All of these solutions have been enabled by the relative accuracy of lithography models, as well as the speed and precision of leading metrology tools and the sheer computational power of modern compute clusters. As we consider the challenges of patterning solutions, it is clear that adopting such computational approaches to the full pattern transfer process will be limited by the speed and especially the accuracy of etch and films simulation capability. Phenomenological models are available and are heavily used to illustrate 3D process flows. However, the accuracy and completeness of etch modeling lags far behind lithography. The difference is best seen by considering model separability.

In lithography simulation[27], we can create a model including mathematical descriptions of an exposure tool, including lens and illumination systems; a reticle; and a resist stack. If we have valid initial data, the model should yield results of comparable quality is we switch out one element of the model – the reticle pattern or the Zernike aberration coefficients, for example – or change discrete input parameters such as film thickness or exposure dose. Model separability is a major reason that lithography simulation can be used to simulate large ranges of parametric variations and make useful predictions for process optimization and control[28].

Etch modeling[29,30], on the other hand, is not easily separable. An etch model is affected by conditions on multiple length scales; the macroscale description of the etch chamber, including pressure, gas flow and temperature variations; mesoscale modeling of the plasma itself with its inherent short time scale variation; and microscale effects due to the interaction of the plasma with the masking pattern. Changing the conditions of any of these interrelated components may render the results highly inaccurate. In this respect, etch modeling tends to be highly descriptive of a particular process, but it is lacking in the predictive capability needed for process control.

It is certainly not surprising that etch simulation is not as predictive as lithography. The plasma environment is significantly more chaotic than the relatively well behaved world of photons and photosensitive molecules. Even the evolving need for stochastic simulation in the lithography domain is significantly simpler than the three dimensional controlled chaos of an etch chamber. The number of different chemical pathways available for reaction within an etcher

can also present a daunting challenge. The etch process actually needs these multiple pathways to passivate sidewalls while etching vertically in order to carefully balance lateral vs. vertical etch rates and provide the desired material selectivity.

Etch faces additional challenges due to the resist pattern itself. Over the years, resist films have been reduced in thickness to such an extent that the resist itself is no longer adequate to act as the transfer mask for the entire etch process. Etch stacks are now a complex layer cake of optical materials (anti-reflection coatings) and multiple hard masks. While this simplifies the resist patterning process, it has shifted the burden to etch, making the stack more complex and difficult to model. Etch recipe optimization remains largely the domain of highly talented and diligent engineers whose work is often more an art than a science.

Finally, etch modeling is complicated by variations in the resist or other patterns being used as the transfer mask. Three dimensional roughness of the resist sidewall results in a net averaging during etch, and any tendency of the guide pattern towards non-vertical profiles will affect the rate at which the reactive species can enter and exit the narrow openings in the pattern. This is especially evident in SADP where the spacers often have one vertical and one rounded edge, and they may even lean in towards their neighbors due to a lack of structural integrity. Multiple patterning is also susceptible to pitch walking, where the gaps between lines vary in an alternating cadence. These localized variations have a clear impact on the final etch profile (Fig. 4).

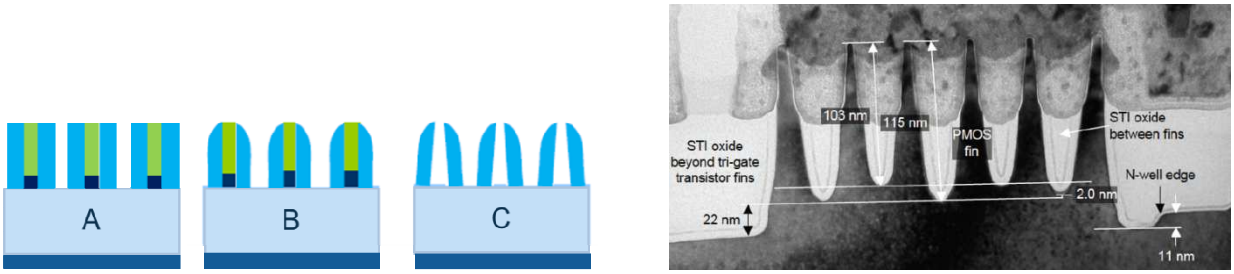

Figure 4: Left: Idealized SADP profiles (A) vs. rounded sidewalls (B) and showing the effect of pattern deformation (C). Right: Actual cross sections showing alternating etch depths following a multiple patterning process (photo courtesy of ChipWorks).

Despite these challenges, significant progress has been made in etch modeling. Tool suppliers make extensive use of macroscale simulation to develop new chambers and processes, and modeling can be used to accelerate cycles of learning. Leading researchers in the "plasma-to-profile" community are hopeful that they can reach the level of predictive modeling that has been achieved in lithography. Developing first principles etch simulators to rival lithography programs is beyond the scope of this conference, and it would certainly be an odd message for the introductory talk in this session to focus on this topic exclusively. But better predictive models are possible using today's etch framework, even if the models need to be tuned for each specific process. One of the keys is incoporating etch data into OPC modeling at an early stage of development. While OPC should, in principle, include etch proximity effects, this is difficult to implement in practice as the process itself is not locked down. While the effort would be significant, driving patterning solutions below the 10 nm node is worth the effort to perform more post-etch characterization as early as possible in the development cycle, and to keep it updated through fast cycles of learning. One area of emphasis should be improved 3D metrology to minimize the unknowns in the transfer process.

4. PREDICTIVE CONTROL IN PATTERNING SOLUTIONS: "HOLISTIC PATTERNING"

One of the key lessons from the success of a holistic approach to lithography[31] is the power and value of predictive control. The ability to measure selected metrology data and combine it with tool data and simulation to predict optimal process corrections improves the quality of wafer output and maximizes efficiency and productivity. This concept should logically be extended to the full patterning process, creating holisitc patterning solutions.

One key to any holistic solution is to be able to merge measurements and models to generate more net results and more actionable responses than what were actually measured. If we measure X data points and can confidently predict what we would have measured at 10 times as many locations, or if we measure N parameters and can predict N+1 outputs, we can begin to appreciate the power of such holistic combinations. It is interesting to note that the opposite of holism is

defined as reductionism, which is, in many ways, the essence of traditional engineering. We are, collectively, very good at breaking complex problems into pieces and solving each piece separately. We have specialized conferences on specific subjects, and it is a mark of esteem in this industry to be known as "the" expert in a specific area. The core principle of holistic solutions is exactly the opposite, moving back towards generalism and wide ranging expertise. Patterning solutions drive the need for generalists rather than specialists, and for combining disparate data from multiple sources to reach the optimal solution, even if the knobs we must turn to reach that solution are not those traditionally used by lithographers.

With or without improved etch modeling, tighter control is possible using neural networks and other machine learning strategies to make us of the massive amounts of data generated by process tools, as well as the full depth of metrology data – not just individual measured parameters but also metrics of measurement quality, similarity to expected signal shapes and even image quality data. Feedback and feed forward control loops incorporating this broad range of data can help push patterning solutions forward, but they require imagination and invention.

Consider edge placement errors as an example. If we only measure a few CD and overlay targets per wafer it would be difficult to predict the complex EPE distribution for many different types of features produced in a multiple patterning scheme. But if we add in image based data from a wide field SEM, scatterometry spectra and film thickness data, a more complete model could be computed. We should also consider the addition of non-traditional data streams such as e-beam or optical defect inspection data or wafer shape parameters, all combined to build up a more detailed 3D model of what has happened to the entire wafer during the process cycle.

The use of stress measurements for predictive control of overlay errors has recently emerged as a novel use of a tool not ususally associated with patter wafer metrology[32]. However, as tolerances shrink, it is clearly necessary to develop new ways to model and predict process induced variations. In the overlay case, the connection between stress induced in a thermal anneal process and 2D overlay is fairly simple to model, and is indicative of the power of predictive control when metrology and process variations are studied throughout the process.

5. METROLOGY CONSIDERATIONS FOR PATTERNING SOLUTIONS

Another key to the creation of holistic patterning solutions is the study and implementation of optimized sampling plans[33],[34]. Simply measuring a fixed number of points at preset locations on a few wafers may easily miss critical process excursions. Numerous options exist to use our limited number of available measurements more effectively by combining multiple sources of data. Process tool log files and trace data provide key indcators of process and tool stability that are just beginning to be used effectively. If we parse these files in real time to detect tool drift or even single wafer anomalies, we can more readily detect and identify excursions in time, collect additional data to determine the nature and root cause of the excursion, and, more importantly, take corrective action to recover process stability. Examples include laser power and bandwidth data down to the pulse by pulse level, wafer focus and leveling data, alignment signal strength, and in-situ conditions within an etch or deposition chamber.

The ability to adapt sampling plans while a lot is in process clearly depends on the automation system running production within a fab. In many cases it is difficult to change the timing of a metrology recipe or reroute lots for additional measurement without disrupting the flow of wafers in production. But if data exists and can be used to improve output quality and die yield it is certainly worth the effort to identify the most promising potential applications of adaptive sampling plans and put them to use.

6. CONCLUSIONS

The trend towards continued device shrinks through patterning processes rather than steadily shrinking resist dimensions will only continue to accelerate. Even as EUV nears production readiness it is already nearly at the limit of single exposure capability; the expense of multiple patterning EUV solutions will require even more attention to cost and manufacturability of these solutions. The optical lithography conference, while no longer the dominant event at this symposium, remains the best central venue for sharing ideas and developments across the entire range of lithographic and patterning challenges.

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