

# PROCEEDINGS OF SPIE

## ***VLSI Circuits and Systems VI***

**Teresa Riesgo**  
**Massimo Conti**  
*Editors*

**24–26 April 2013**  
**Grenoble, France**

*Sponsored and Published by*  
SPIE

**Volume 8764**

Proceedings of SPIE 0277-786X, V. 8764

SPIE is an international society advancing an interdisciplinary approach to the science and application of light.

VLSI Circuits and Systems VI, edited by Teresa Riesgo, Massimo Conti, Proc. of SPIE Vol. 8764,  
876401 · © 2013 SPIE · CCC code: 0277-786X/13/\$18 · doi: 10.1117/12.2031867

Proc. of SPIE Vol. 8764 876401-1

The papers included in this volume were part of the technical conference cited on the cover and title page. Papers were selected and subject to review by the editors and conference program committee. Some conference presentations may not be available for publication. The papers published in these proceedings reflect the work and thoughts of the authors and are published herein as submitted. The publisher is not responsible for the validity of the information or for any outcomes resulting from reliance thereon.

Please use the following format to cite material from this book:

Author(s), "Title of Paper," in *VLSI Circuits and Systems VI*, edited by Teresa Riesgo, Massimo Conti, Proceedings of SPIE Vol. 8764 (SPIE, Bellingham, WA, 2013) Article CID Number.

ISSN: 0277-786X

ISBN: 9780819495617

Published by

**SPIE**

P.O. Box 10, Bellingham, Washington 98227-0010 USA

Telephone +1 360 676 3290 (Pacific Time) · Fax +1 360 647 1445

SPIE.org

Copyright © 2013, Society of Photo-Optical Instrumentation Engineers.

Copying of material in this book for internal or personal use, or for the internal or personal use of specific clients, beyond the fair use provisions granted by the U.S. Copyright Law is authorized by SPIE subject to payment of copying fees. The Transactional Reporting Service base fee for this volume is \$18.00 per article (or portion thereof), which should be paid directly to the Copyright Clearance Center (CCC), 222 Rosewood Drive, Danvers, MA 01923. Payment may also be made electronically through CCC Online at [copyright.com](http://copyright.com). Other copying for republication, resale, advertising or promotion, or any form of systematic or multiple reproduction of any material in this book is prohibited except with permission in writing from the publisher. The CCC fee code is 0277-786X/13/\$18.00.

Printed in the United States of America.

Publication of record for individual papers is online in the SPIE Digital Library.



[SPIDigitalLibrary.org](http://SPIDigitalLibrary.org)

---

**Paper Numbering:** Proceedings of SPIE follow an e-First publication model, with papers published first online and then in print and on CD-ROM. Papers are published as they are submitted and meet publication criteria. A unique, consistent, permanent citation identifier (CID) number is assigned to each article at the time of the first publication. Utilization of CIDs allows articles to be fully citable as soon as they are published online, and connects the same identifier to all online, print, and electronic versions of the publication. SPIE uses a six-digit CID article numbering system in which:

- The first four digits correspond to the SPIE volume number.
- The last two digits indicate publication order within the volume using a Base 36 numbering system employing both numerals and letters. These two-number sets start with 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B ... 0Z, followed by 10-1Z, 20-2Z, etc.

The CID Number appears on each page of the manuscript. The complete citation is used on the first page, and an abbreviated version on subsequent pages. Numbers in the index correspond to the last two digits of the six-digit CID Number.

# Contents

- vii *Conference Committee*
- ix *Introduction*
- xi *An autonomous structural health monitoring solution (Plenary Paper) [8763-501]*  
C. A. Featherston, K. M. Holford, R. Pullin, J. Lees, M. Eaton, M. Pearson, Cardiff Univ. (United Kingdom)
- xvii *Biologically inspired large scale chemical sensor arrays and embedded data processing (Plenary Paper) [8763-502]*  
S. Marco, A. Gutiérrez-Gálvez, Univ. de Barcelona (Spain) and Institute for Bioengineering of Catalonia (Spain); A. Lansner, Kungliga Tekniska Högskolan (Sweden); D. Martinez, Ctr. National de la Recherche Scientifique (France); J. P. Rospars, Institut National de la Recherche Agronomique (France); R. Beccherelli, Consiglio Nazionale delle Ricerche (Italy); A. Perera, Univ. Politècnica de Catalunya (Spain); T. Pearce, Univ. of Leicester (United Kingdom); P. Vershure, Univ. Pompeu Fabra (Spain); K. Persaud, The Univ. of Manchester (United Kingdom)

---

## SESSION 1 ANALOG CIRCUIT DESIGN

---

- 8764 02 **A 2.5 Gb/s low-voltage CMOS fully-differential adaptive equalizer [8764-1]**  
C. Gimeno, E. Guerrero, C. Aldea, S. Celma, Univ. de Zaragoza (Spain)
- 8764 03 **Reducing flicker noise up-conversion in a 65nm CMOS VCO in the 1.6 to 2.6 GHz band [8764-2]**  
F. Pepe, A. Bonfanti, S. Levantino, C. Samori, A. L. Lacaita, Politecnico di Milano (Italy)
- 8764 04 **Rectennas design using DG-MOSFETs [8764-33]**  
R. Rodríguez, B. González, J. García, M. Marrero-Martín, A. Hernández, Univ. de Las Palmas de Gran Canaria (Spain)
- 8764 05 **Energy harvesting with piezoelectric applied on shoes [8764-4]**  
E. Camilloni, M. Carloni, M. Giammarini, M. Conti, Univ. Politecnica delle Marche (Italy)
- 8764 06 **A 1.2 V low-power OpAmp for integrated lock-in amplifiers [8764-5]**  
M. R. Valero, S. Celma, N. Medrano, B. Calvo, C. Gimeno, Univ. de Zaragoza (Spain)

---

## SESSION 2 MULTIMEDIA APPLICATIONS

---

- 8764 07 **FPGA-based implementation for steganalysis: a JPEG-compatibility algorithm [8764-6]**  
E. Gutierrez-Fernandez, M. Portela-García, C. Lopez-Ongil, M. Garcia-Valderas, Univ. Carlos III de Madrid (Spain)

- 8764 08 **Implementation of scalable video coding deblocking filter from high-level SystemC description** [8764-7]  
P. P. Carballo, O. Espino, R. Neris, P. Hernández-Fernández, T. M. Szydzik, A. Núñez, Univ. de Las Palmas de Gran Canaria (Spain)
- 8764 09 **Network-on-chip emulation framework for multimedia SoC development** [8764-9]  
G. Singla, F. Tobajas, V. de Armas, Univ. de Las Palmas de Gran Canaria (Spain)

---

**SESSION 3 MODELING AND SIMULATION**

---

- 8764 0A **Protocol-level noise analysis of networked systems based on simulation/analytical approach** [8764-10]  
G. B. Vece, E. Mazza, M. Conti, Univ. Politecnica delle Marche (Italy)
- 8764 0B **A simulation technique to compute phase noise induced from cyclostationary noise sources in RF oscillators** [8764-11]  
F. Pepe, A. Bonfanti, S. Levantino, P. Maffezzoni, C. Samori, A. L. Lacaita, Politecnico di Milano (Italy)
- 8764 0C **An IOMMU for hardware-assisted full virtualization of heterogeneous multi-core SoCs** [8764-12]  
G. Kornaros, K. Harteros, M. Astrinaki, I. Christoforakis, Technological Educational Institute of Crete (Greece); M. Coppola, STMicroelectronics (France); M. D. Grammatikakis, Technological Educational Institute of Crete (Greece)

---

**SESSION 4 SIGNAL PROCESSING**

---

- 8764 0E **A low-cost PSoC architecture for long FFT** [8764-14]  
P. A. Lomoio, P. Corsonello, Univ. della Calabria (Italy)
- 8764 0F **High speed Radix-4 soft-decision Viterbi decoder for MB-OFDM UWB system** [8764-15]  
G. Liang, J. Portilla, T. Riesgo, Univ. Politécnica de Madrid (Spain)
- 8764 0G **A comparative study of continuous-time analog adaptive equalizers** [8764-17]  
C. Sánchez-Azqueta, C. Gimeno, S. Celma, Univ. de Zaragoza (Spain)

---

**SESSION 5 RECONFIGURABILITY AND VIRTUALIZATION (DREAMS)**

---

- 8764 0H **Architectural evaluation of dynamic and partial reconfigurable systems designed with DREAMS tool** [8764-18]  
A. Otero, Á. Gallego, E. de la Torre, T. Riesgo, Univ. Politécnica de Madrid (Spain)
- 8764 0I **Virtual platform for power and security analysis of wireless sensor network** [8764-19]  
A. Díaz, J. Gonzalez-Bayon, P. González de Aledo Marugán, P. Sanchez, Univ. de Cantabria (Spain)

- 8764 OJ **A hierarchical scheduling and management solution for dynamic reconfiguration in FPGA-based embedded systems** [8764-20]  
T. Cervero, A. Gómez, S. López, R. Sarmiento, Univ. de Las Palmas de Gran Canaria (Spain); J. Dondo, F. Rincón, J. C. López, Univ. de Castilla-La Mancha (Spain)
- 8764 OK **Efficient and decentralized data transfer architecture for component based embedded systems** [8764-21]  
D. de la Fuente, J. Barba, J. Dondo, F. Rincón, M. J. Santofimia, J. C. López, Univ. de Castilla-La Mancha (Spain)

---

**SESSION 6 TEST AND TECHNOLOGY**

---

- 8764 OL **Hardening digital systems with distributed functionality: robust networks** [8764-22]  
A. Vaskova, M. Portela-Garcia, M. Garcia-Valderas, C. López-Ongil, Univ. Carlos III de Madrid (Spain); J. Portilla, J. Valverde, E. de la Torre, T. Riesgo, Univ. Politécnica de Madrid (Spain)
- 8764 OM **Fault tolerant architectures by partial reconfiguration** [8764-23]  
L. A. Cardona, Instituto de Microelectrónica de Barcelona (Spain) and Univ. Autònoma de Barcelona (Spain); Y. Guo, Instituto de Microelectrónica de Barcelona (Spain); C. Ferrer, Instituto de Microelectrónica de Barcelona (Spain) and Univ. Autònoma de Barcelona (Spain)
- 8764 ON **Introduction on performance analysis and profiling methodologies for KVM on ARM virtualization** [8764-24]  
A. Motakis, A. Spyridakis, D. Raho, Virtual Open Systems (France)
- 8764 OO **OPC mask simplification using over-designed timing slack of standard cells** [8764-25]  
Y. Qu, C. H. Heng, A. Tay, T. H. Lee, National Univ. of Singapore (Singapore)

---

**SESSION 7 COMMUNICATION AND WSNS**

---

- 8764 OP **A micropower supervisor for wireless nodes with a digital pulse frequency modulator battery monitor** [8764-26]  
M. Carloni, Univ. Politecnica delle Marche (Italy); R. d'Aparo, P. Scorrano, B. Naticchia, SmartSpace Solutions (Italy); M. Conti, Univ. Politecnica delle Marche (Italy)
- 8764 OQ **Wireless sensor network for wide-area high-mobility applications** [8764-27]  
I. del Castillo, R. Esper-Chaín, F. Tobajas, V. de Armas, Univ. de Las Palmas de Gran Canaria (Spain)
- 8764 OR **Intelligent microchip networks: an agent-on-chip synthesis framework for the design of smart and robust sensor networks** [8764-28]  
S. Bosse, Univ. Bremen (Germany)
- 8764 OS **STAR: FPGA-based software defined satellite transponder** [8764-29]  
D. Davalle, R. Cassettari, S. Saponara, L. Fanucci, Univ. di Pisa (Italy); L. Cucchi, Intecs S.p.A. (Italy); F. Bigongiari, W. Errico, Sitael S.p.A. (Italy)

- 8764 OT **Design and optimization of an RF energy harvesting system from multiple sources** [8764-35]  
M. Ali, L. Albasha, N. Qaddoumi, American Univ. of Sharjah (United Arab Emirates)

---

**POSTER SESSION**

---

- 8764 OU **Transmission line pulse system for avalanche characterization of high power semiconductor devices** [8764-30]  
M. Riccio, G. Ascione, G. De Falco, L. Maresca, M. De Laurentis, A. Irace, G. Breglio, Univ. degli Studi di Napoli Federico II (Italy)
- 8764 OV **State of the art direct digital frequency synthesis methodologies and their performance on FPGA** [8764-31]  
M. Genovese, E. Napoli, Univ. degli Studi di Napoli Federico II (Italy)
- 8764 OX **MPPM system for indoor wireless optical communications with angle-diversity detection** [8764-34]  
A. García-Viera, S. Rodríguez, B. R. Mendoza, O. González, A. Ayala, Univ. de La Laguna (Spain)
- 8764 OY **Processor core for real time background identification of HD video based on OpenCV Gaussian mixture model algorithm** [8764-8]  
M. Genovese, E. Napoli, Univ. degli Studi di Napoli Federico II (Italy)

*Author Index*

# Conference Committee

## *Symposium Chair*

**Thomas Becker**, EADS Innovation Works (Germany)

## *Symposium Cochairs*

**Christos Tsamis**, National Center for Scientific Research Demokritos  
(Greece)

**Gerhard Krötz**, University of Applied Sciences in Kempten (Germany)

## *Symposium Local Chair*

**Marc Belleville**, CEA-Leti (France)

## *Conference Chair*

**Teresa Riesgo**, Universidad Politécnica de Madrid (Spain)

## *Conference Cochair*

**Massimo Conti**, Università Politecnica delle Marche (Italy)

## *Conference Programme Committee*

**Eduard Alarcon**, Universidad Politècnica de Catalunya (Spain)

**Marco Caldari**, Korg (Italy)

**João Canas Ferreira**, Universidade do Porto (Portugal)

**Marcello Coppola**, STMicroelectronics (France)

**Eduardo de la Torre-Arnanz**, Universidad Politécnica de Madrid (Spain)

**Valerio Frascolla**, Intel GmbH (Germany)

**Mohammed Ismail**, Khalifa University of Science, Technology and  
Research (United Arab Emirates)

**George Kornaros**, Technological Education Institute of Crete (Greece)

**Jose Francisco Lopez Feliciano**, Universidad de Las Palmas de Gran  
Canaria (Spain)

**Celia López-Ongil**, Universidad Carlos III de Madrid (Spain)

**Mar Martínez**, Universidad de Cantabria (Spain)

**Natividad Martínez**, Reutlingen Universität (Germany)

**Salvador Mir**, TIMA Laboratoire (France)

**Pere Lluís Miribel-Català**, Universidad de Barcelona (Spain)

**Simone Orcioni**, Università Politecnica delle Marche (Italy)

**Ioannis Papaefstathiou**, Technical University of Crete (Greece)

**Jorge Portilla**, Universidad Politécnica de Madrid (Spain)

**Franco Ripa**, Korg (Italy)

**Ángel B. Rodríguez-Vázquez**, Universidad de Sevilla (Spain)

**Ruben Salvador**, Universidad Politécnica de Madrid (Spain)

**Sergio Saponara**, Università di Pisa (Italy)  
**Roberto Sarmiento Rodríguez**, Universidad de Las Palmas de Gran Canaria (Spain)  
**Ralf Seepold**, Hochschule Konstanz (Germany)  
**Walter Stechele**, Technische Universität München (Germany)  
**Christian Stehno**, CoSynth GmbH & Co. KG (Germany)  
**Fabian Vargas**, Pontificia Universidade do Rio Grande do Sul (Brazil)  
**Alisson Vasconcelos de Brito**, Universidade Federal da Paraíba (Brazil)

*Session Chairs*

- 1 Analog Circuit Design  
**Teresa Riesgo**, Universidad Politécnica de Madrid (Spain)
- 2 Multimedia Applications  
**Roberto Sarmiento Rodríguez**, Universidad de Las Palmas de Gran Canaria (Spain)
- 3 Modeling and Simulation  
**Concepción Aldea**, Universidad de Zaragoza (Spain)
- 4 Signal Processing  
**Stefan Bosse**, Universität Bremen (Germany)
- 5 Reconfigurability and Virtualization (DREAMS)  
**Marta Portela-García**, Universidad Carlos III de Madrid (Spain)
- 6 Test and Technology  
**Marcello Coppola**, STMicroelectronics (France)
- 7 Communication and WSNs  
**Massimo Conti**, Università Politecnica delle Marche (Italy)



## Introduction

The book you have in your hands contains the papers presented at the sixth edition of the Conference on VLSI Circuits and Systems, embedded in SPIE's Microtechnologies event. Once again, you have the opportunity to read excellent research works covering different topics in the field of electronic systems design and technology, integration, etc.

Browsing the proceedings of previous editions of the conference, one can observe the rapid evolution of topics in this field, which are directly followed by the event every two years. Many of the works directly related with VLSI design are focused to the analog and mixed-signal area, where there is still much work to do to make the designers' lives easier. On the other hand, many of the papers related with digital systems are focused on complex architectures based on Many-Cores, Network-on-Chip, with special attention to aspects such as reconfigurability and reliability. There are still many research opportunities in modeling, simulation, testability and power efficiency in both aspects, analog and digital. Applications where complexity is an issue, like multimedia, communications and signal processing, are still challenging and newer aspects of system design, like wireless sensor networks, appear on stage to show us how the electronic designers are interested in applications that involve different technologies and disciplines.

As conference chairs, we would like to thank all the authors, chairs and attendees for their contribution to the event. Special thanks to the program committee members who have helped us a lot in the paper selection and session setup. Many thanks to SPIE staff for their continuous support, patience, and help in editing this book.

We hope to meet you soon, in two years more or less, and let's work together to make the future event as successful as this one.

**Teresa Riesgo**  
**Massimo Conti**