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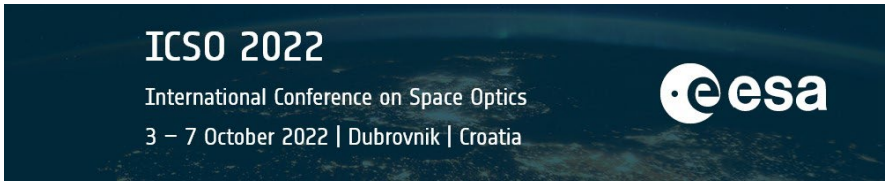

Innovations in visible imaging technology to support future space missions.

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Innovations in visible imaging technology to support future space missions.

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ABSTRACT

Teledyne e2v is continuing to invest in CCD and CMOS sensors innovation for higher performance in the visible, soft X-Ray and NIR parts of the spectrum for space applications. Space missions are becoming ever more complex and Teledyne e2v, to support this growth, has developed technologies to improve the intrinsic performance of the detector, new features for low noise or data stream approach and improved interfaces to ease integration at system level. As Teledyne also covers commercial and industrial markets it is possible to take advantages of the state-of-the-art development made in those markets to enhance detector performance for space with limited risk and shorter R&D development time.

This paper covers the latest innovations for CCD and CMOS technologies and in particular the large area and low noise platform (CIS300 family) and TDI charge domain CIS125. In the last section an overview on the detector electrical interface innovation is given.

Keywords: Innovation, CCD, CMOS, high speed, ultra-low noise, HiRho, NIR, TDI charge domain, electrical interface.

1. INTRODUCTION

Advances in imaging solutions are a key contributor to commercial semiconductor growth. This is due to the increasing use of visible imaging technology in many applications. Space imaging is also experiencing a rapid growth, especially in New Space markets where the detectors are at the centre of many systems. This growth takes advantage of the advances in commercial technology to enable more complex missions with ever reducing development timescales.

The route to support such rapid evolution is to innovate on technologies for higher intrinsic detector performance, more features and increased electronic integration. Teledyne-e2v presents the results covering the latest innovations for CCD, CMOS detectors.

We present results on a new CCD for space mission: the coronagraph detector on the Nancy Grace Roman Space telescope, which will represent the first used of an electron multiplication CCD (EMCCD) in a major space mission. In addition, large area CCDs continue to be used when large arrays are required, for example in SMILE.

CMOS image sensor are now used for the majority of space missions and continue to offer both improved performance and features. Three CMOS imagers and their measured performance will be presented with a focus on noise performance. CIS300 a large area 9k x 8.6k 10 µm pixel pitch detector featuring high speed, high dynamic range and ultra-low noise technology enabling sub electron performance. CIS220 a HiRho version of CIS120 (selected for ESA's CO2M Copernicus mission) with a significant increase of the QE times MTF figure of merit in Near-Infra-Red with a QE of 60% at 950nm and an MTF of 0.55. CIS125 is the latest product from the TDI charge domain family for high resolution earth observation with high full well capacity of 30 ke^- from a 5 µm pixel pitch.

The last section will cover electrical interface choices which play a key part in determining the complexity of integration of the detectors with the focal planes and front end electronics.

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2. CCD TECHNOLOGY

CCD technology remains an important part of the detectors delivered by Teledyne-e2v for space missions. In the section an update on two more recent programs are presented: EMCCD for NASA's Nancy Grace Roman Space Telescope and CCD for soft X-ray astronomy applications SMILE.

2.1 EMCCD (electron multiplying CCD) for space science and astronomy

The CCD311-20 has been developed for use in the Coronagraph in NASA's Nancy Grace Roman Space Telescope (RST, formerly known as WFIRST). The CCD311-20 is largely based on the CCD301-20 test chip, which itself was a variant of Teledyne e2v's commercial CCD201-20 sensor. The CCD201-20 is a frame transfer EMCCD with an active imaging area of 1024 x 1024 13µm square pixels, designed for back-side illumination. For the RST CGI the back-surface light shield is removed from what was previously the store section, which allows the bottom half of the pixel array to be used for imaging. The key features of the CCD311-20 are summarized in Table 1 and more information on the sensor development and characterization can be found in Harding et al. [1].
For the test chip design and characterization test activities, the CCD311 has the following changes from the CCD301 test chip design:

- All active pixels have been modified to one design from the four implemented on the CCD301 test chip, with a 3 µm notch channel centred within a 9 µm wide buried channel. This was added for improved CTE performance after irradiation.
- Previously closed channels in the isolation region between the multiplication register and overspill register have been opened up to control the level of charge under the RØ1 electrodes.
- The overspill register, which receives this excess charge, is re-routed to a dump drain instead of recombining with the primary register run-off leading to the output node. This was employed to reduce the sensitivity to cosmic rays.

Table 1: EMCCD CCD311-20 key features.

Parameter	**CCD311-20**
Array size	2048 rows by 2048 columns
Pixel size	13 µm by 13 µm
Operational Mode	NIMO (IMO available)
Multiplication gain	x7500 gain demonstrated In photon counting, NIMO (VSS=0V) mode, x4000 gain is sufficient to amplify at least 90% of the events over the five-sigma threshold. (This is because the CCD + system noise is less than 90 electrons.)
Serial register	1 serial register with an output amplifier on each end – the EM output with low responsivity for readout through the multiplication register and a second (non-EM output) with high responsivity at the opposite end of the serial register
Full well capacity	Image: 58 ke-, Register: 100 ke-, Output node: 1,200 ke- (multiplication channel), 264 ke- (high responsivity)

The CCD qualification phase of the program for RST CGI is complete with the production test phase due to start imminently.

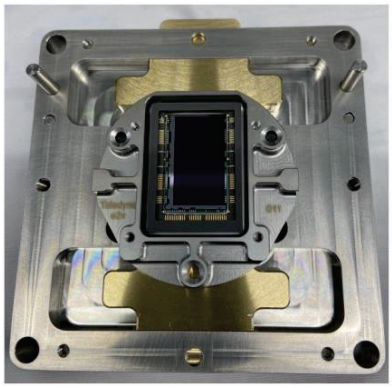


Figure 1: Photo of the EMCCD CCD311-20 in its handling jig.

2.2 CCD for soft X-ray astronomy applications - SMILE

The Solar wind Magnetosphere Ionosphere Link Explorer (SMILE) is a soft X-ray mission observing photon energies of 200 eV to 2000 eV. This mission is a collaboration between ESA and Chinese Academy of Science [2]. For this mission the Teledyne e2v CCD370 has been selected. To minimise the CCD CTI degradation due to proton radiation impact, the focal plane has a temperature control to below -100°C. The CCD characteristics are given in Table 2 along with the schematic of the CCD370 in Figure 2.

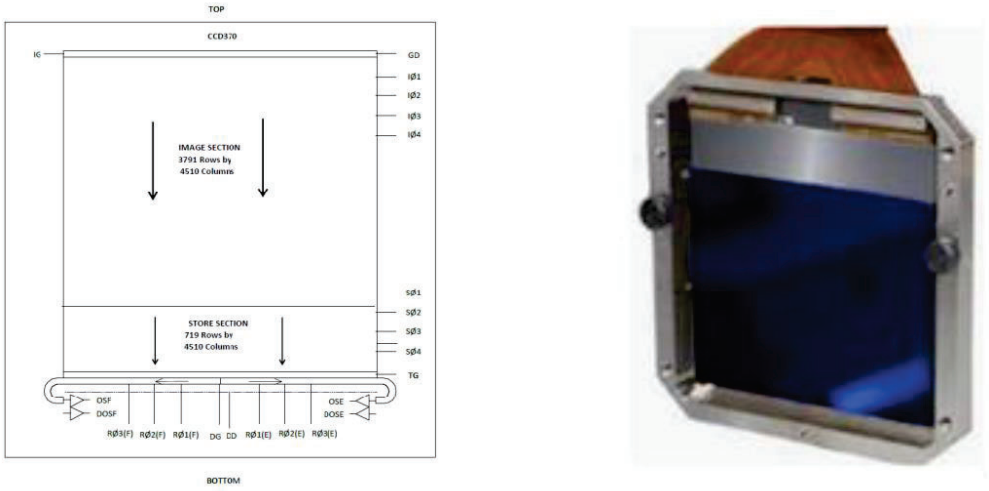


Figure 2: CCD370 schematic on the left and in its handling jig for the SMILE program on the right.

Table 2: CCD370 main characteristics.

Parameter	Typical Characteristic	Units
Array image section	3791 rows x 4510 columns	N/A
Array store section	719 rows x 4510 columns	N/A
Pixel pitch	18 x 18	µm
Peak Charge Storage (Image/ store)	850 (note 1)	ke-/pixel
Peak Charge Storage (register or output)	660 (register) 400 (output)	ke-/pixel
Output amplifier responsivity	7	µV/e-
Readout noise	13 (note 2)	e-RMS
Dark signal at 203k	0.5	e-/pixel/s
Quantum Efficiency at -70 °C, at 900 nm	>15	%

Notes:
1- When operating with two adjacent phases held high. Defined as the point at which the response is non-linear. Measured using flat-field illumination.
2- Calculated with a camera bandwidth of 15 MHz predicted with single ended readout.
The detector used for the PLATO mission, CCD280, has been used to predict the CCD370 post radiation performance [3]. The results show that the CCD370 will meet the end-of-life performance when the temperature is kept below -85 °C. Figure 3 (figure 13 from [3]) shows the CTI performance post annealing.

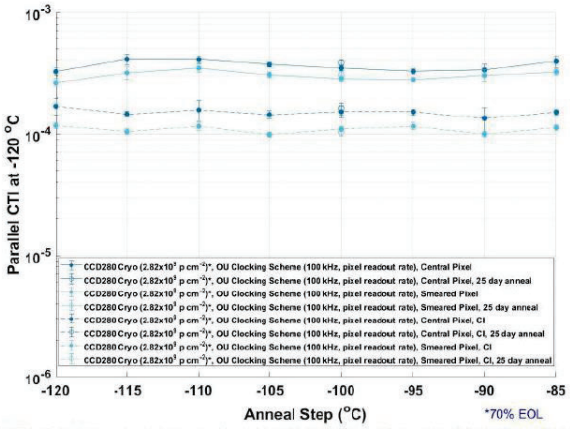


Figure 13: Impact of temperature annealing on X-ray parallel CTI with and without one line of 8500 e⁻ charge injection. Plot also shows the parallel CTI after a 25 day anneal at -120 °C, after warming up to -100°C

Figure 3: CTI performance post annealing [3].

The program is now moving to the lot acceptance testing (LAT) phase for flight model (FM) delivery.
The SMILE mission has the capability to cool the image sensor down to cryogenic temperatures during evaluation testing to correctly evaluate the CCD end-of-life performance.

3. LARGE AREA CMOS DETECTOR DEVELOPMENT

3.1 Large area CMOS development from Teledyne e2v

Teledyne e2v has developed a new CIS300 family of CMOS detectors to specifically address astronomy, space, low noise and high dynamic range applications while being a platform that can be adapted with minimum risk for many other specific applications. Teledyne e2v has completed the design of the first two products from this family: CIS301 and CIS302, which is the high NIR sensitivity version of CIS301 using the HiRho technology. This platform is the results of years of R&D innovation re-using silicon proven blocks from various projects. The key innovations that will be discussed in this section are:

- Large area
- Low noise
- Improved distribution of key pixel performance
- High QE x MTF figure of merit especially in Near Infra-Red

CIS300 a flexible large area detector platform

The CIS301 is a large area backthinned CMOS image sensor in a 3-sided close buttable package (See Figure 4 and Figure 5). It features:

- 9,000 columns and 8,600 rows of 10µm x 10µm, selectable dual gain pixels
- Capable of rolling shutter, global shutter and High Dynamic Range (HDR) Operation
- Selectable 12 bit or 14 bit operation (effectively extendable by HDR)
- High frame rates from 12 CML outputs each running at 2Gbit/s
- Region Of Interest (ROI) feature enabling fast access to small pixel areas of interest
- High quantum efficiency (QE) from Teledyne's world leading backthinning processing
- Designed for use over a wide range of temperatures - room to cryogenic temperature
- Silicon Carbide and Ceramic precision package
- Onboard Temperature Sensors

The CIS302, second product of the family, is the HiRho version of the CIS301:

- Enhanced sensitivity
- Enhanced near infrared performance while maintaining high modulation transfer function (MTF) performance
- All other features the same

Package designed to be 3-side buttable (Figure 5).

- 2 mm dead space between adjacent image areas
- Designed to operate at temperatures from +25°C to -100°C
- Image area flatness per sensor < 25 µm typical peak-to-valley at -100°C (based on the distance between two closest parallel planes that encompass the full image area.)
- Height tolerance per sensor of ±15 µm through use of precision shims (based on variation between best fit image area plane and best fit plane between the 3 shim interface surfaces)

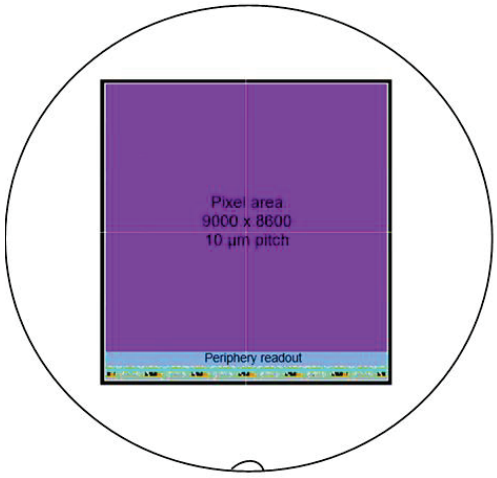


Figure 4: CIS302 wafer scale – top level layout view.

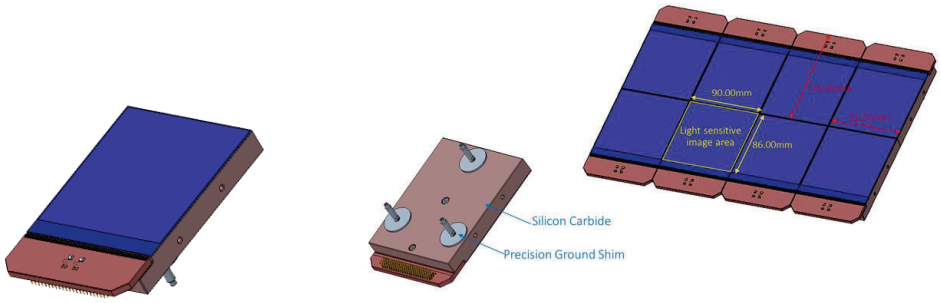


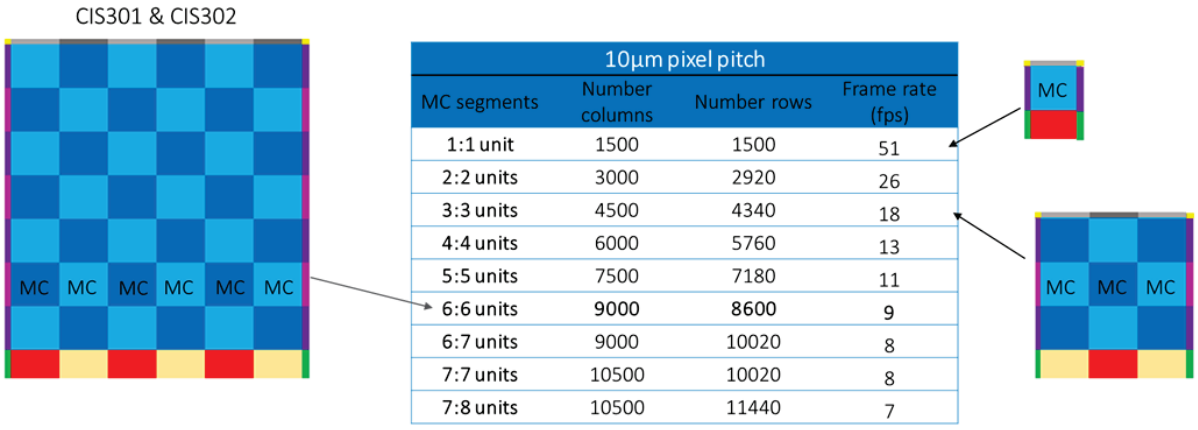
Figure 5: CIS301/CIS302 package and focal plane array (FPA) arrangement example.

The detectors predicted performance are reported in Table 3. The family is built on a 2D stitch platform which enables different detector sizes to be manufactured with the same mask set as shown Figure 6. Further the column readout for the family is based on a 5µm pitch making the platform suitable for pixel pitches of 5µm and larger.

Table 3: Performance CIS301 and CIS302 detectors.

Parameters	**CIS301 and CIS302**
Pixel pitch	10 µm
Array size	9000 columns x 8,600 rows
Pixel type	Pinned Photodiode, Switchable dual gain
Operating Modes include	Rolling Shutter HDR (High Dynamic Range) Global Shutter Staircase (multiple non-destructive reads)
ADC bits	Selectable 12 or 14 bits
Frame rate	8 fps @12 bits (Rolling shutter) 8 fps max @ 12 bits (Simple Global shutter) 4 fps max @ (Global Shutter with Digital Double Sampling (DDS))
Region of Interest	Capable of selecting region of interest in row and column directions - freedom to select any or all combinations of adjacent odd and even rows - can select from the 12 outputs to use to select different groups of columns

Multiple Gain settings	Any combination of pixel and pre-amplifier gain: Pixel gain: x1, x10 Pre-Amplifier gain: x1, x3, x7, x15, x31
Full Well Capacity	> 140 ke$^-$ (lowest pixel gain setting) > 15 ke- (highest pixel gain setting)
Noise	< 2 e$^-$ (high gain rolling shutter) < 5 e$^-$ (high gain global shutter) < 30 e$^-$ (low gain rolling shutter)
Dynamic Range with HDR operation	95dB typical
QE @550nm	95% (dependent on anti-reflection coating)
Dark Current	0.01e-/s @-50°C Dark current halves for every reduction of 5-6°C
Interface	12 CML outputs 50 MHz Master Clock SPI
Package/chip format	Three side buttable, silicon carbide package
Power Dissipation	6 W (at full frame rate) Low power mode exists (down to < 2W).



10µm pixel pitch			
MC segments	Number columns	Number rows	Frame rate (fps)
1:1 unit	1500	1500	51
2:2 units	3000	2920	26
3:3 units	4500	4340	18
4:4 units	6000	5760	13
5:5 units	7500	7180	11
6:6 units	9000	8600	9
6:7 units	9000	10020	8
7:7 units	10500	10020	8
7:8 units	10500	11440	7

Figure 6: CIS301 and CIS302 format variant using the same mask set.

The CIS300 platform has been built on the heritage of silicon proven blocks and technologies. The low noise approach in particular was important and was addressed by 5 design considerations (represented Figure 7):

- Achieving a high CVF, above 80 µV/e$^-$
- Use of a column amplifier
- Improvement of pixel sensitivity and in-pixel gain distribution
- Implementation of ultra-low noise in pixel source follower
- Integration of specific low noise modes such as non-destructive readout and multi-sampling

These 5 points are the focus of the next sections.

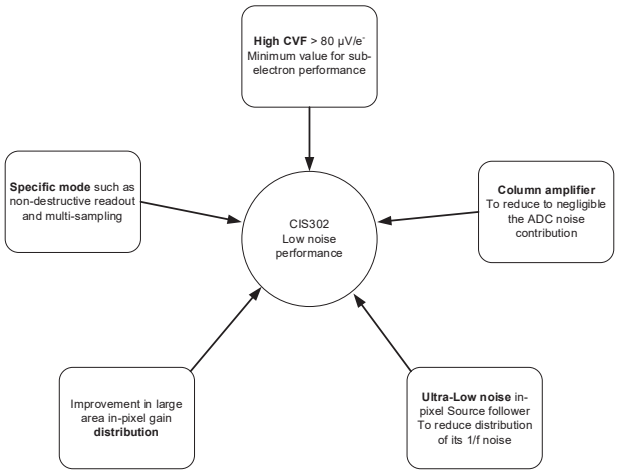


Figure 7: CIS302 - low noise approach.

3.2 Large area with High CVF

To achieve noise floor below 2 e^-_{RMS} CIS300 family relies on a high gain of 80-90µV/e^- at sense node. This is higher than the typical achievable value from standard imaging process which is more around 50-60µV/e^-. In order to reach 80-90µV/e^- some specific design technics must be considered. Although several generations of detectors have achieved these high values a summary of the technics used for CIS300 is presented below.

In order to achieve 80-90µV/e^- three main considerations have been looked at:

- Reduction of sense node capacitance by reducing the minimum sense node area and adjusting the implant to further reduce the reverse bias parasitic diode capacitance.
- Use of the smallest reset transistor connected to the sense node. This usually needs improvement in noise performance to not produce an intrinsic reset noise increase.
- The optimization of the transfer gate shape to minimize its parasitic capacitive contribution to the sense node while not affecting the lag performance.

The high CVF brings a lower sense node FWC as a consequence. It was therefore important to design a reset scheme and ADC to enable the largest possible voltage swing at the sense node by:

- Use of overdrive to reset the sense node with the highest voltage possible for the technology chosen.
- To have the largest ADC input common mode voltage.

Although this does not impact the noise performance it helps with dynamic range by optimizing the FWC.

The first large area high CVF and low noise CMOS detector demonstrated by Teledyne e2v is the CIS113, developed as part of the TAOSII mission [4]. This was a large area CMOS detector (1920 x 4608 Pixels of 16µm square) with low noise, below 3 $e^-_{RMS,}$ and a reasonable FWC of 20 ke^-. The pixel was a 5T structure similar to CIS300 pixel.

The CIS113 was used in cryogenic environment which enabled the assessment of performance across a wide temperature range. The figures below shows that CVF increases (Figure 9) with lower temperature while the noise floor in electron remains constant (Figure 10). This is explained by the fact that the 1/f noise appears first as a current from the in-pixel source follower that is integrated into the column and sense node capacitances. As the temperature reduces the noise in µV increases (Figure 10) proportionally to the decrease of the sense node capacitance (or increase of the CVF) keeping the ratio of CVF increase to noise in µV constant. The implication is that the optimum sizing for the in-pixel source follower is in relation between its parasitic capacitance and the sense node targeted capacitance. Further detail can be found in [5]. Note that CIS113 is now a device in production.

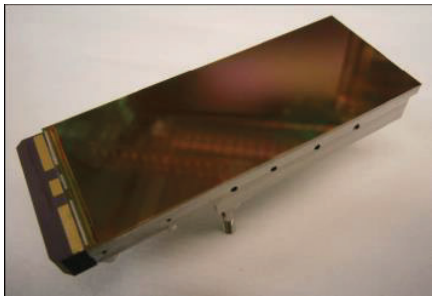


Figure 8: CIS113 large area (pixel array of about 3.1cm x 7.4cm) and low noise CMOS detector.

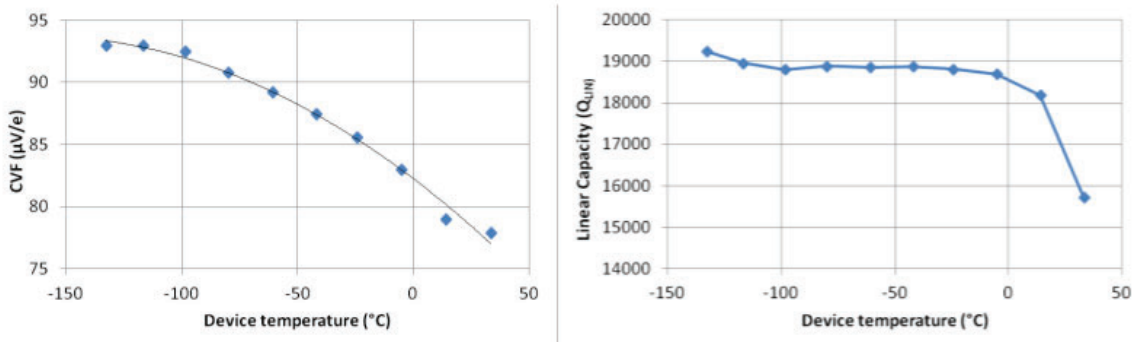


Figure 9: CIS113 CVF and Linear charge capacity versus temperature.

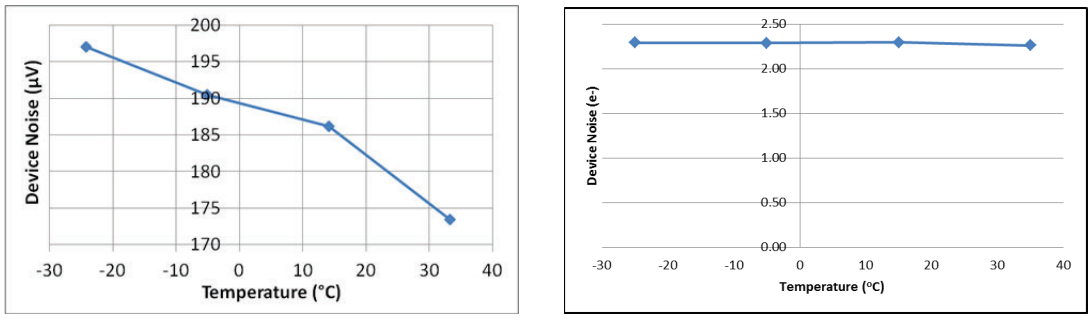


Figure 10: CIS113 noise performance versus temperature: left noise in µVRMS and right in e-RMS.

Having increased the gain as much as possible (using standard design rules) within the technology and design capabilities the next step was to improve the in-pixel CVF distribution across the large pixel area. This has been achieved with the implementation of HiRho technology, which along with improving QE and MTF significantly improves the in-pixel gain distribution

3.3 Enhanced sensitivity and improved in-pixel gain distribution

The sensitivity of the device is also an important characteristic of photon starved applications especially for NIR and soft X-ray missions. Teledyne e2v has already successfully transferred the CCD back thinning capability to CMOS and more recently has implemented of its HiRho CMOS technology. The pixel of the CIS300 family has been designed with this technology.

A weak point of CMOS technology is the photodiode depletion depth which is smaller in comparison to the CCD. This is due to the fact that CMOS uses lower voltages. This lack of deep depletion implies that once back thinned the total thickness cannot exceed around 10 µm without a strong MTF degradation, even when using high resistivity epitaxial material. This limits the QE in NIR. The HiRho technology addresses this dilemma. This technology consists of supplying a negative voltage, named reverse bias, to the back surface while preventing the transistor from leaking [6]. Figure 11 shows a representation where the Deep Depletion Extension (DDE) is a special implant added in the pixel to protect the in-pixel transistors from the reverse bias.

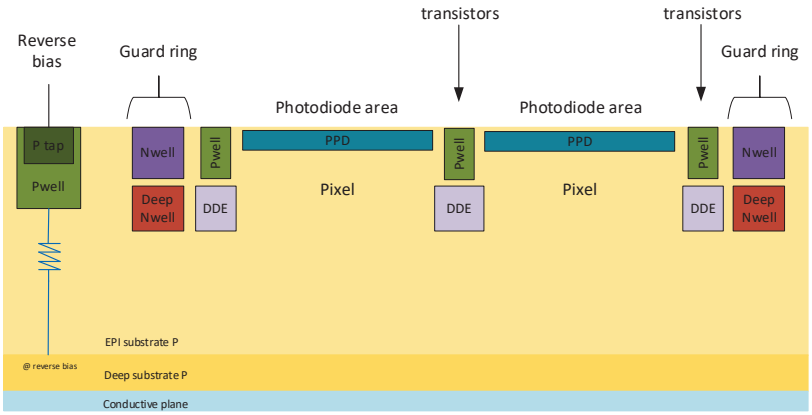


Figure 11: HiRho – 2 pixels reverse bias in-pixel DDE protection representation.

This technology has been implemented successfully as part of a European Space Agency GSTP funded program. The device designed (CIS22) is a HiRho version of the CIS120 general multi-purpose detector, 2k x 2k, 10 µm pitch, 5T pixel with global and rolling shutter operation. This device has been selected for ESA's Copernicus CO2M mission) [7]. The QE and MTF have been measured for two EPI thicknesses of 17 µm with -6 V reverse bias, and 33 µm with -20 V reverse bias, see Figure 12 and Figure 13. The MTF is almost a constant across the wavelengths which demonstrates full depletion, although the values are slightly lower than the perfect theoretical value and slightly lower for the 33 µm thickness compared to 17 µm. This is explained by the aspect ratio between the pixel pitch of 10 µm and the thicknesses (17 µm and 33 µm). Some electrons can escape the pixel depletion region due to lateral diffusion to be captured by a neighbouring pixel. Nevertheless, these results show an important sensitivity increase in the NIR compared to the CIS120 non-HiRho detector. The QE response of CIS220 is significantly higher at wavelengths above 700 nm and almost double from 850 nm onwards for the 33 µm thick device compared to the CIS120. Importantly MTF performance of the CIS220 is not compromised by using thicker silicon and is improved compared to CIS120. It is worth pointing out that as the QE roll off appears later, the fringing effect is reduced improving performance for narrow wavelength bandwidth applications like hyperspectral imaging or spectroscopy. This is another important key point of this technology.

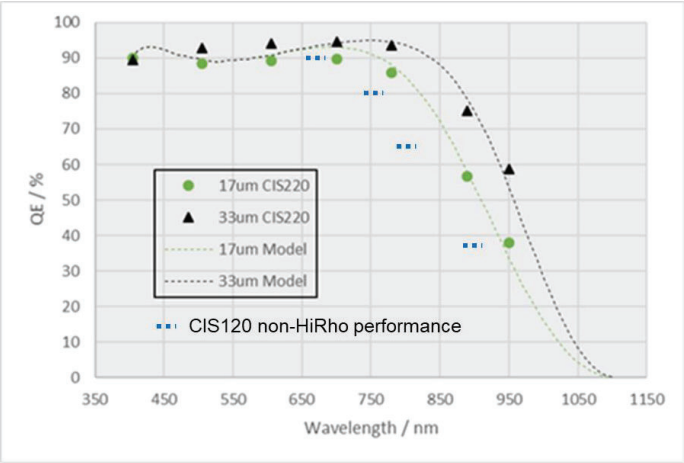


Figure 12:CIS220 HiRho QE response for two thicknesses and comparison with non-HiRho CIS120 thinned to 9µm.

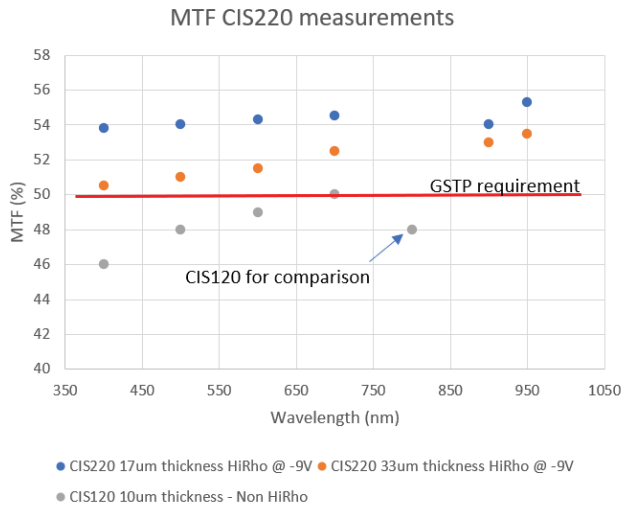


Figure 13: CIS220 HiRho MTF response for two thicknesses.

The in-pixel gain distribution of the HiRho device is also significantly improved. The CCF (Charge Conversion Factor, digital equivalent of CVF for analogue devices) has a much tighter distribution. This is key for large area devices and critical for sub electron performance. Figure 14 reports a comparison between the distribution of CCF for CIS120 (non-HiRho) and CIS220 (HiRHo with 17µm thick EPI). A substantial improvement of 2 to 3 can be observed. The two devices have been tested on the same camera using the same analysis software.

Further CIS220 was expected to have a good Parasitic Light Sensitivity (PLS) performance as it is using thick material (17µm EPI) and it is fully depleted. The left graph Figure 15 indicates that PLS performance in percent is constant up to saturation level and after this point the PLS increases. This right graph Figure 13 shows a decrease of PLS performance with longer wavelength which is expected as the device is back illuminated and therefore at longer wavelength the electrons are generated too close to the sense node. The observation can be categorized as:

- Up to 600nm the PLS ratio is better than 1 to 4000
- From 600nm to 890 nm the PLS ratio is better than 1 to 1000
- From 890nm to 950nm the PLS ratio is better than 1 to 667

Note that CIS220 is targeting to close TRR in coming months. A campaign of radiation is planned by end 2022.

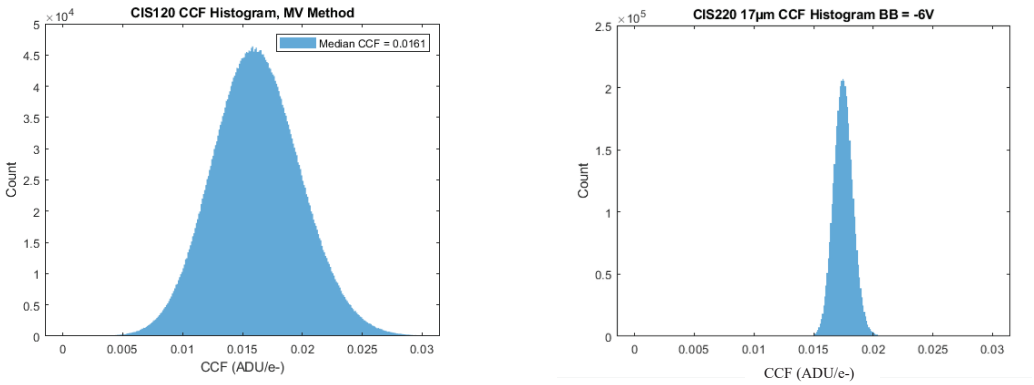


Figure 14: HiRho impact on CCF distribution: left CIS120 (non-HiRho) and right CIS220 (HiRho).

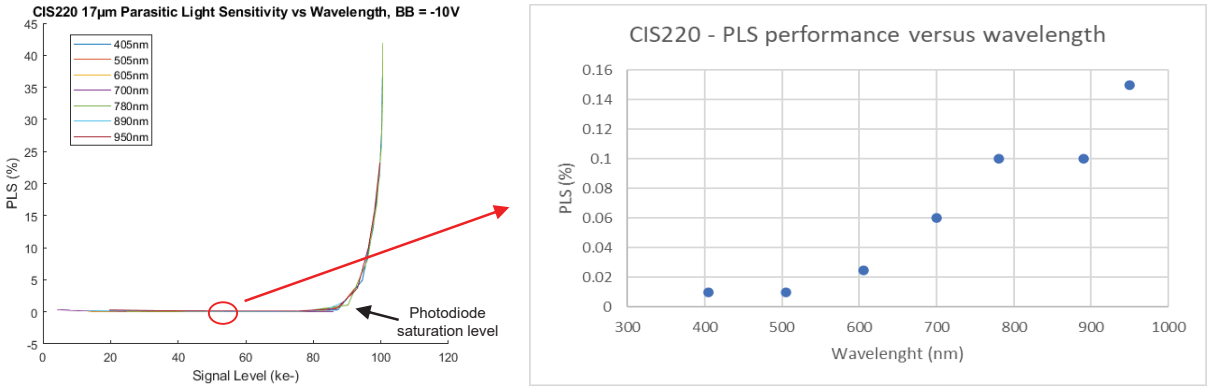


Figure 15: CIS220 PLS perfromance versus signal level (left) and wavelength right.

3.4 Column amplifier and Ultra-Low noise in-pixel source follower:

Figure 16 is an illustration of a typical readout out digital path with a column PGA (Programmable Gain amplifier). For the CIS300 family the gains proposed varies from x 1 (bypass), x 2 to x 31. A similar approach was already used successfully on CIS124 [8]. This is a large array detector of 800 x 800 4T pixel, with low noise (3 e^-_{RMS}) and high frame rate (700 fps) designed for the ELT program as a wavefront sensor for ESO. Since the noise target was below 3 e^-_{RMS} PGA in this case had a gain of only up to x 8. However, as the CIS300 family is targeting a noise floor below 2 e^-_{RMS} and even sub electron in some mode the gains of the PGA needed to be increased. The choice of gains is also a function of

the ADC noise floor. Here we have implemented a single slope ADC from industrial application optimized and featuring a noise floor below 100 μV_{RMS}. Between the PGA and ADC a correlated double sampling (CDS) circuit is used to remove KTC noise and very low frequency and very high frequency noise components as the CDS acts as a bandpass filter.

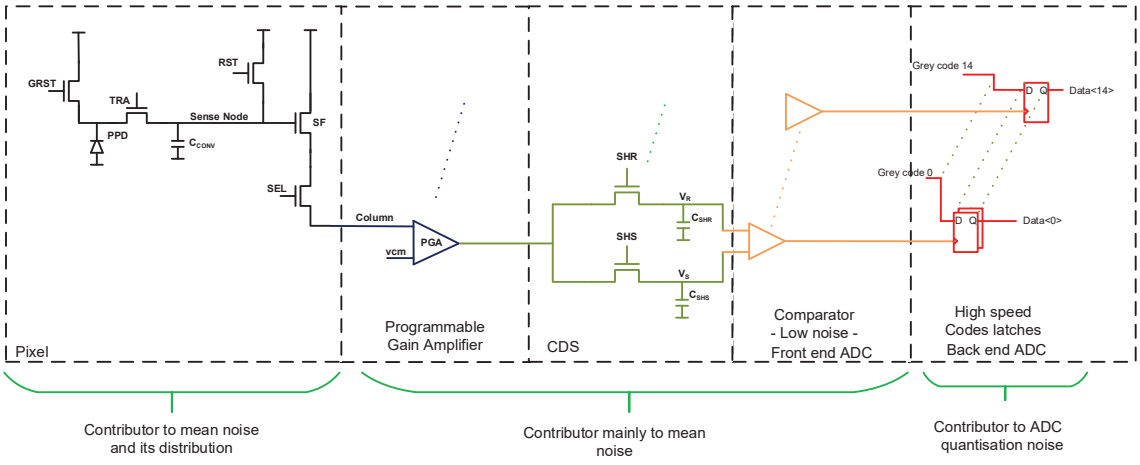


Figure 16: Readout path with top level view of timing and noise contributions.

Figure 17 reports CIS124 noise floor versus PGA gain showing a significant noise reduction. Note that CIS124 is now in its production phase.

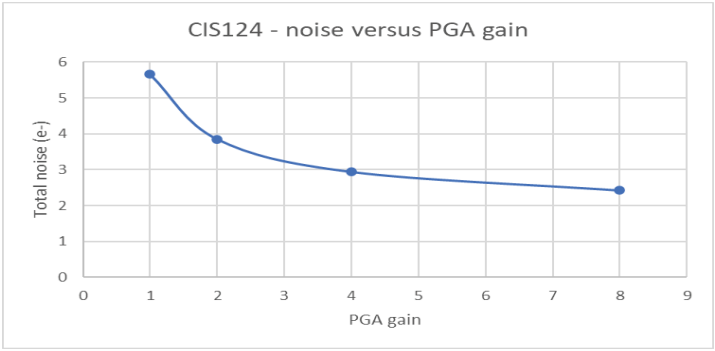


Figure 17: CIS124 noise floor versus PGA gain.

To fully take advantage of the high CVF, the reduction of in-pixel gain distribution and column PGA structure it was important to have a tighter in-pixel source follower noise distribution. A new structure called ultra-low noise has been successfully experimented on silicon. Figure 18 shows a significant improvement in the noise tail. Further we can see a mean value measured at 1.6 e^-_{RMS} with a modest CVF of 70µV/e^-. This value is now low enough to target sub electron performance using non-destructive readout or multi-sampling technics.

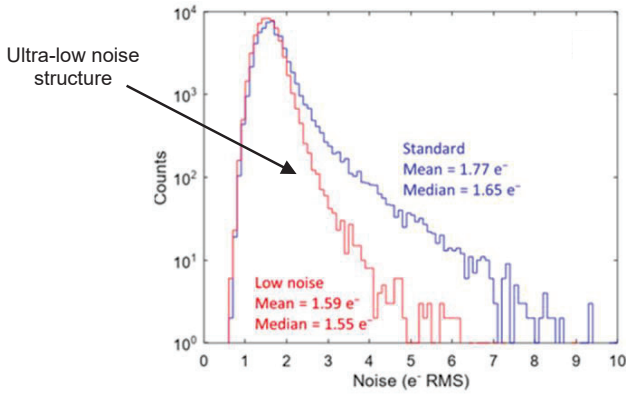


Figure 18:Performance of pixel with ultra-low noise process (in red) compared to low noise process (in blue) obtained with a CVF of 70µV/e- [9].

The CIS300 family targets a noise floor close to 1.6 e^-_{RMS} using high CVF, in-pixel ultra-low noise source follower with a tight distribution and a column amplifier to render the ADC readout noise negligible. The non-destructive read out or multi-sampling will further reduce the noise floor to achieve sub electron performance. These modes can be important features for applications where long integration time is used and where cosmic ray artefacts must be removed for instance. However, more work is required to choose the best option between non-destructive read out and multi-sampling. In CMOS technology non-destructive read out relys on building-up a voltage at the sense node. This node is not pinned and its dark current is significantly higher than the dark current of the photodiode. This might be a limitation post radiation and a multi-sampling approach with sub electron performance might be preferred in some applications.

4. TDI CHARGE DOMAIN

The Earth Observation satellites uses linear TDI (Time delay integration) detectors to maximise the level of signal gathered in order to achieve the required signal-to-noise ratio (SNR) to at low ground sampling distance (GSD). In this section an update is reported on CIS125 a 5µm pixel pitch TDI charge domain CMOS detector.

A testchip was first developed to establish the performance of TDI charge domain pixels of 5µm and 7µm pixel pitch with anti-blooming included. The first use of such pixel was for the development of CIS125 (Figure 19). This device development started under a CEOI EO Technology and Instrumentation Program funded by the UK Space Agency. And it has now has been selected as part of the ESA InCubed funding stream. The architecture developed is reported in Figure 20. This TDI charge domain detector is composed of 4 panchromatic (PAN) bands and 6 multi-spectral (MS) bands. The configuration reported here is optimised and each PAN and MS are composed of sub-TDI bands (A&B) that to enhance the full well by adding off-chip digital summation to the charge domain performance. The PAN and MS number of TDI lines were carefully chosen to optimise application needs versus silicon area. Each sub-TDI needs to be read out separately and therefore needs its own conversion. This is the equivalent of reading out 16 independent bands. This implies that each quarter of line is dedicated to the conversion of a 1 PAN and 1 MS as shown Table 4. More information on the implementation of this device can be found in [10].

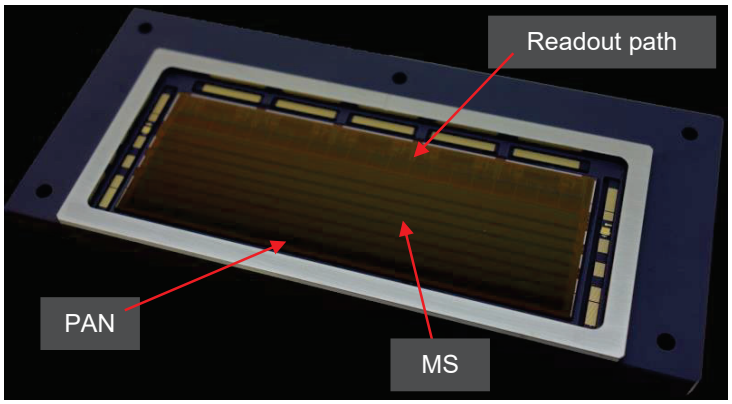


Figure 19: CIS125 device in its package.

The pixel, Figure 21, is a 4 phases (P1…P4) CCD structure, with gated anti-blooming (AB). This sensor is a stitched device with 16k columns for the PAN bands and 8k columns for the MS bands. The pixels are 5µm square and for the PAN band and 10µm square for the MS band, see Table 1. To speed up the frame rate the sensor uses a high speed ADC per column allowing 12 bits conversion in 0.9µs. This is a single slope ADC architecture with a counter generating ten gray codes and four phase-shifted unary codes providing 12 bits output in total at very high line rates. The column readout path is illustrated Figure 18. A single read path is shared between all bands to implement a maximum number of bands without the need of 2D stitching technology and optimising power consumption. The data resulting of the image conversion is then sent to a gigabit transmitter (GTX) composed of a serialiser working in double data rate mode (DDR) at 3.6 GHz operation and a Common Mode Logic (CML) data driver working at 2.8 Gb/s. The high speed CML output driver standard has been selected to minimize the number of outputs reducing the complexity of any associated front end electronics. Input signals such as clock, integration control and SPI interface use LVDS format.

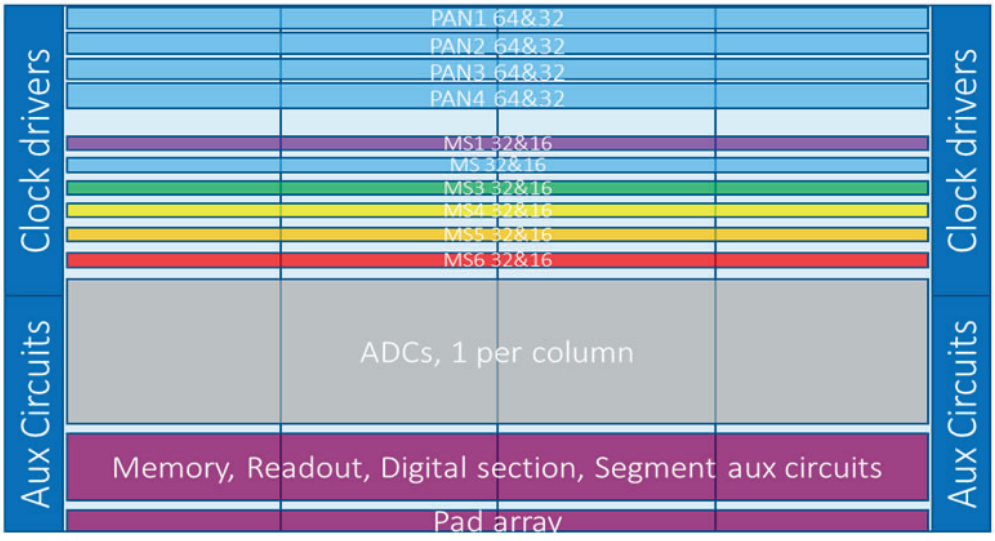


Figure 20: CIS125 architecture top level diagram.

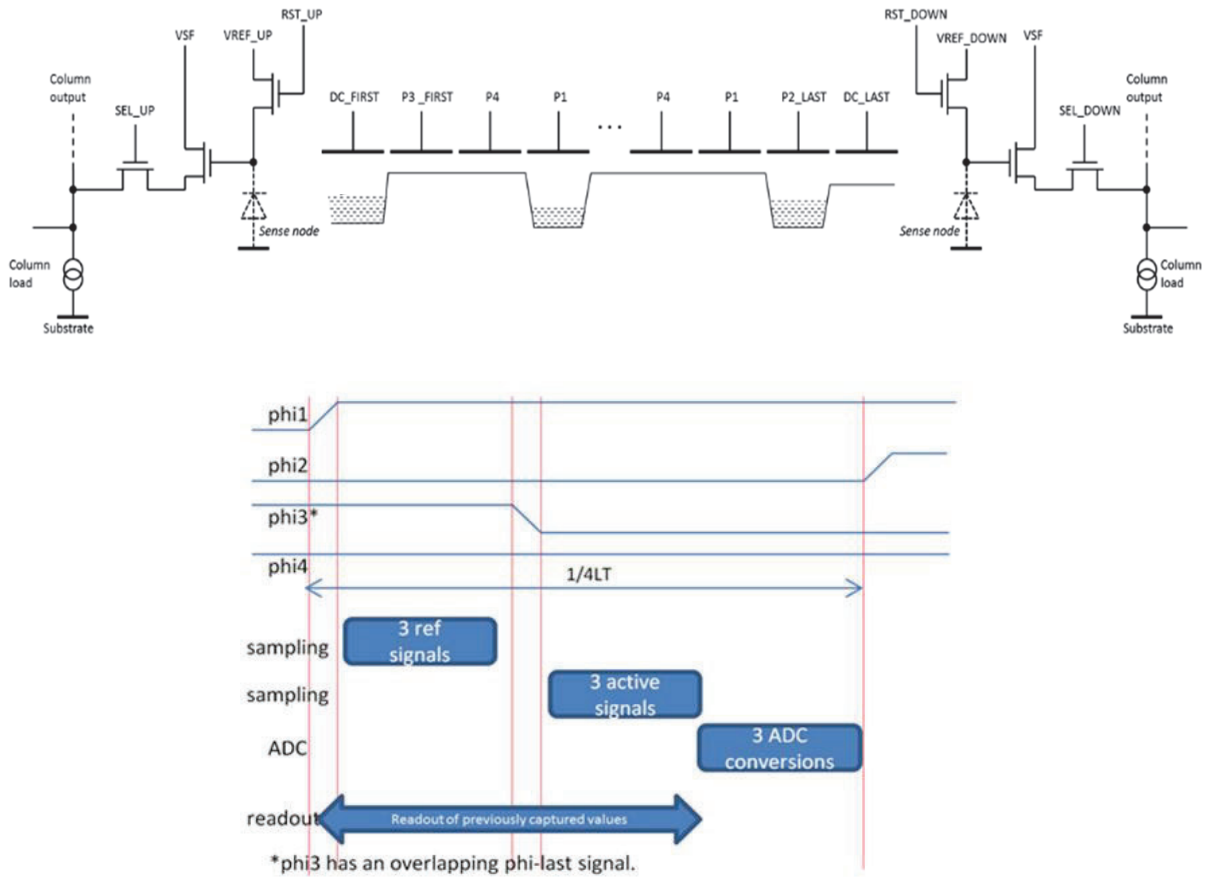


Figure 21: 4 phases TDI pixel schematic at the top and phase timing diagram at the bottom.

Table 4: Configuration for CIS125.

Pixel count		Pixel size (µm)	
PAN	MS	PAN	MS
16k	8k	5	10

Table 5: PAN and MS readout timing organisation.

1/4LT			1/4LT			1/4LT			1/4LT		
P1A	P1B	MS1A	P2A	P2B	MS1B	P3A	P3B	MS2A	P4A	P4B	MS2B

1/4LT			1/4LT			1/4LT			1/4LT		
P1A	P1A	MS3A	P2A	P2B	MS3B	P3A	P3B	MS4A	P4A	P4B	MS5B

A key parameter for CMOS TDI technology is the Charge Transfer Inefficiency (CTI) performance. This also indicates the maximum FWC of the pixel before the pixel changes from a buried channel operation to surface Channel. The latter is not preferred in space applications because the post radiation degradation will affect the CTI and hence MTF performance. This is not the case for a pixel working in buried channel mode only. In this section the author will refer the FWC obtained in buried channel operation as CTI FWC and a FWC obtained in surface channel operation as saturation FWC.

The pixel was initially designed and optimised on a testchip. This testchip also included a 7 µm pixel version. Results are given in Figure 22 of the CTI curves with FWC associated obtained on both 5µm and 7µm pixel pitch of the testchip using a back illuminated version, backthinned down to about 12µm. CLK_HIGH is the high voltage of the phase (P1…P4). This voltage is adjusted for best CTI FWC.

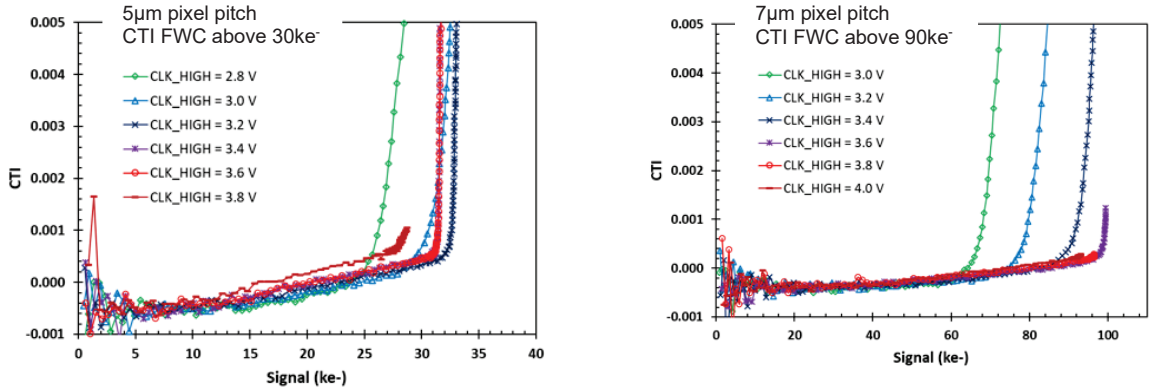


Figure 22: CTI and FWC associated for 5µm pixel pitch (left) and 7µm pixel pitch (right).

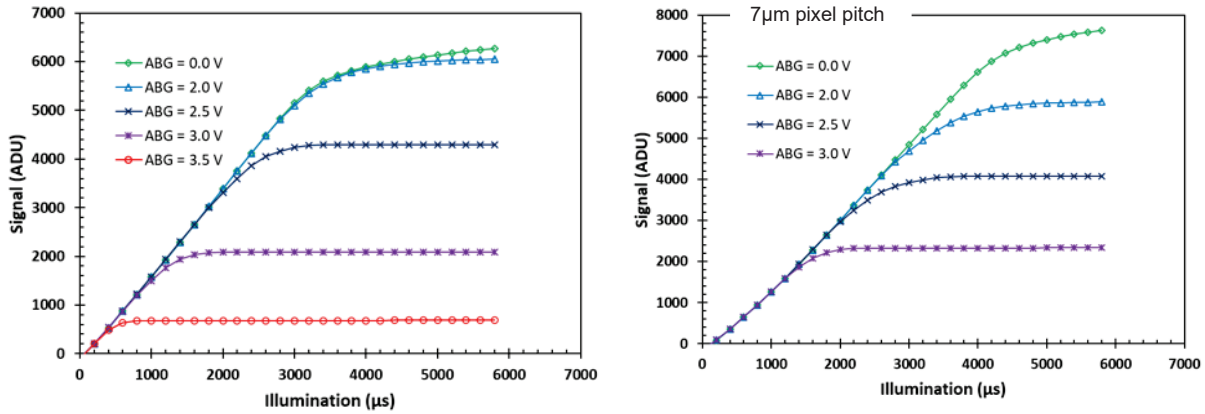


Figure 23: Anti-blooming versus ABG control value for 5µm pixel pitch (left) and 7µm pixel pitch (right).

Preliminary performance of 5µm pitch PAN and 10µm pitch MS of CIS125 confirms the good results from the testchip.

The Figure 24 shows preliminary silicon measurements from the CIS125 PAN1A channel:

- Photon Transfer Curve (PTC) data
- The PTC shows a saturation FWC of approximately 45ke$^-$
- The CTI FWC is approximately 30ke$^-$ (this is the point at which the variance starts to drop off)
- Noise is approximately 30e$^-_{RMS}$ (from the fit to the PTC)

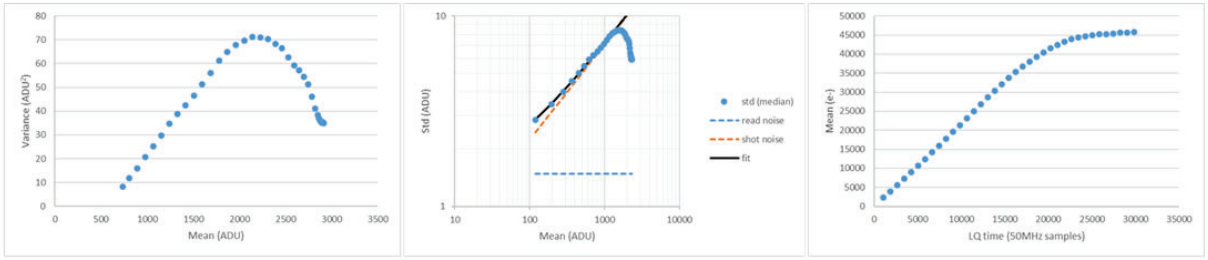


Figure 24: CIS125 PAN1A measurement: mean variance (left), noise (middle) PTC (right)

The Figure 25 shows the silicon measurements done of the MS1A from CIS125:

- Photon Transfer Curve (PTC) data
- The PTC shows a saturation FWC of greater than 150ke$^-$
- The CTI FWC is approximately 110ke$^-$ (this is the point at which the variance starts to drop off)
- Noise is approximately 120e$^-_{RMS}$ (from the fit to the PTC)

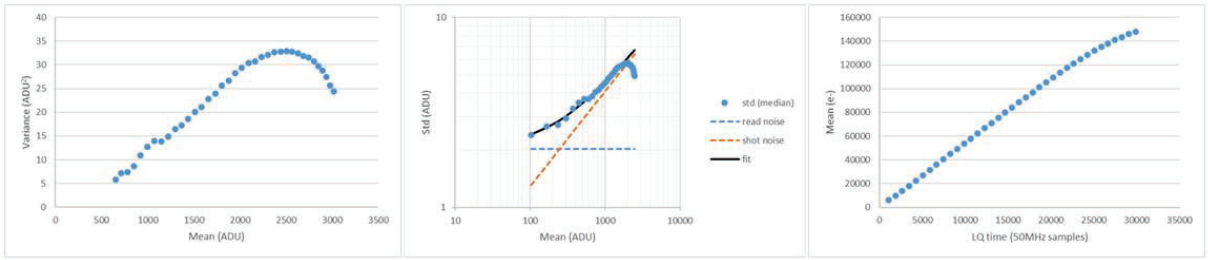


Figure 25: CIS125 MS1A measurement: mean variance (left), noise (middle) PTC (right)

The performance for CIS125 looks very promising with a high CTI FWC of 30 ke$^-$ and saturated FWC of 45 ke$^-$ per PAN channel. Including the digital summation of PAN A and B will bring the CTI FWC to 60 ke$^-$. The CIS125 front illuminated version is expected to be fully characterised by end 2022 and the back illuminated version early 2023.

5. ELECTRICAL INTERFACE

The electrical interface plays a critical role in the design of an image detector since some trade-off depend on it, such as:

- Power consumption,
- Minimizing number of pins per package,
- Maximum data rate hence data handling capability
- Simplifying the detector integration in the system,
- And finally reduce overall cost by a standardization across wide range of products (visible, IR, 2D and linear arrays for instance) simplifying the overall system integration.

For example CIS300, CIS125 or ChromaD (an IR detector from Teledyne [11] selected for instance for ESA's CHIME program) all have implemented a serialiser with CML output standard. This standard enables operation at much higher frequency than LVDS and therefore enables to reduce number of pins (video channels) and static current. This approach will also cover future generation of detector running at faster frame rate with more data to output. Furthermore the CML format can drive meters of cables. This allows large part of the front end electronic to be positioned remotely from the

detector and therefore more protected from radiation. This is obviously interesting for large satellites. In order to ease the integration at high speed and with large volumes of data the output format is of data stream type (Figure 26) and includes per line:

- A word to indicate the start of line (SOL)
- A word to indicate the line (band) readout and other relevant information
- The image data
- Encoding 8b and 10b to guarantee good clock recovery.
- A CRC word
- A word to indicate the end of line (EOL)

Figure 26: Data output format.

This data stream approach includes the clock in the data transmitted removing the need for a clock driver. Further since the clock is simply recovered from the data it removes the problem of the setup and hold constraints between data and clock too small at such high frequency and difficult to master at system level. The encoding 8b and 10b guarantee enough data transition to secure a good clock recovery (Figure 27).

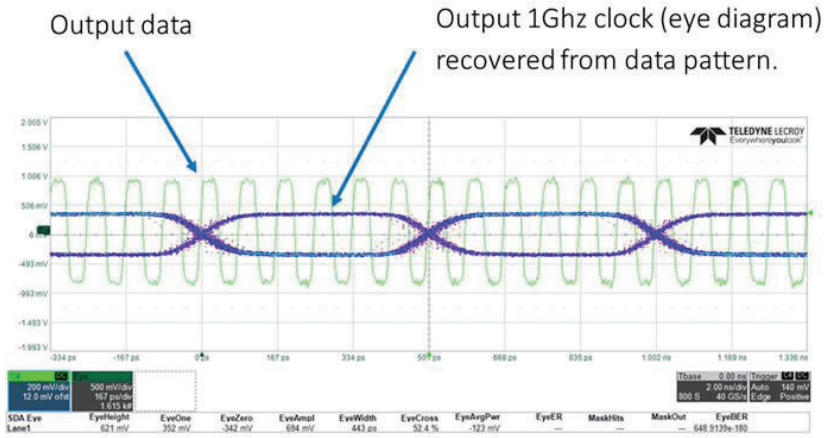


Figure 27: CIS125 1GHz clock recovery example.

6. CONCLUSIONS

Two new CCD have been presented including an EMCCD for the NASA's Nancy Grace Roman Space Telescope. This will be the first EMCCD selected for a space mission. A large CCD for soft X-ray astronomy applications SMILE was also presented.

The large 2D array CMOS detector, 9000 x 8600 with 10 µm 5T pixel pitch, from CIS300 family was presented with a focus on the different technologies used to achieve low noise: high CVF, use of column amplifiers, improved sensitivity and in-pixel gain distribution, implementation of ultra-low noise in-pixel source follower and new features such as non-destructive readout and multi-sampling. The various programs on which these technologies have been verified on silicon were presented indicating a high level of maturity. The HiRho version of the large area array (CIS302) is expected to have a noise floor below 2 e^-_{RMS} with high gain and a FWC of 140 ke^- using a lower in-pixel gain.

The preliminary results of CIS125; a 16k column charge domain TDI 5 µm pixel device with anti-blooming are discussed. The first results confirm the pixel performance with a CTI FWC of 30 ke^- (45 ke^- saturated FWC) per PAN band. Including the digital summation of the paired (A and B) PAN bands gives a CTI FWC of 60 ke^-. This confirms

earlier back illuminated test chip measurements also reported in this document. The results of a 7 µm pixel array on the test chip are also reported, which give a CTI FWC above 90 ke^- per band.
Finally the importance of the electrical interface in saving power and reducing the number of pins while running at higher frame rates and with high data handling capability was discussed.

7. ACKNOWLEDGEMENT

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