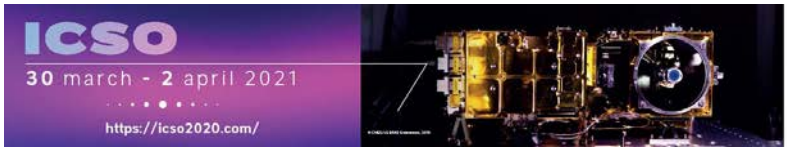
International Conference on Space Optics—ICSO 2020

Virtual Conference

30 March–2 April 2021

Edited by Bruno Cugny, Zoran Sodnik, and Nikos Karafolas



Capella: CIS120 general purpose CMOS sensor for space applications

International Conference on Space Optics — ICSO 2020, edited by Bruno Cugny, Zoran Sodnik, Nikos Karafolas, Proc. of SPIE Vol. 11852, 118520S · © 2021 ESA and CNES
CCC code: 0277-786X/21/$21 · doi: 10.1117/12.2599176

Capella - CIS120 general purpose CMOS sensor for space applications

R. Gil Otero, R. Mackie, C. Greenaway, T. Lemon, P. Jerram, J. Pratlong
Teledyne e2v, 106 Waterhouse Lane, Chelmsford, Essex, England, CM1 2QU

ABSTRACT

Teledyne e2v has developed the Capella CIS120 which is a general purpose CMOS image sensor with high quantum efficiency that has been specifically designed for space applications and it has been selected to be used for the Copernicus Anthropogenic Carbon Dioxide Monitoring (CO2M) mission [1].

We will describe the considerations that led to this CMOS sensor concept and then outline the specifications and design details of this back-illuminated detector. Key features include 2048 × 2048 pixels, 10µm pixel pitch, on-chip ADC giving digital outputs in LVDS format, both rolling shutter and global shutter modes are available, peak Quantum Efficiency (QE) of 90% at 600 nm and latch-up immune and high Single Event Upset (SEU) threshold by design.

We will show how the CIS120 can be used for different modes including multi-linear operation, multi-windowing with independent left and right addressing for star tracker applications for instance and full frame operation in global or rolling shutter mode for array imaging applications including hyperspectral imaging.

We will also present the three different package types have been developed so far for CIS120; standard ceramic package, and sealed Peltier package for space applications and three side buttable metal package for ground base applications.

The CIS120 is designed to be highly flexible in format allowing; larger variants for astronomical applications and multi die focal plane arrangement, a range of backthinning process options and larger pixel sizes for x-ray applications.

The first Capella^{LS}, which is higher pixel full well capacity version, has now being characterized. We will present detailed characterisation and validation results.

Finally, we will summarize plans for future activities including the design and production of a HiRho variant to give significantly improved Near Infra-red (NIR) sensitivity by applying voltage to the back surface to be able to operate in full depletion.

Keywords: High performance visible CMOS sensors, back-illuminated, large full well, Copernicus, Star tracker, hyperspectral, HiRho, Radiation hardness.

1. INTRODUCTION

This paper will start reviewing the different aspects of the die design such as the floorplan and architecture, section 2. Then section 3 will focus on the different operating modes that have been demonstrated and can be used for multiple applications together with the maximum frame rates achieved, 3.1, and also how to configure the sensor to set different integration times 3.2.

Section 4 will briefly describe the three different package developed used and then section 5 will focus on the characterisation results obtained on the first back side illuminated obtained. Also section 6 will present the activities that are being carried out to be able to reach a Technology Readiness Level 6 (TRL6).

Finally, section 7 will present a new variant, CIS220 being developed, CIS220 is the HiRho variant of CIS120, which gives significantly, improved NIR sensitivity.

2. DIE DESIGN OVERVIEW

Table 1 below summarises the top level chip design specifications and Figure 1 shows the Capella CIS120 floorplan with an image area of 2048 × 2048 pixels, 10µm pixel pitch. To avoid any edge effects, the pixel array is surrounded by dummy pixels. Also to allow a close butting package option, and all bond pads are on the bottom edges only.

Table 1. CIS120 Chip Design Specification.

Parameter	Typical value
Number of pixels	2048 x 2048
Pixel size	10 µm
Die size (width x height)	22.2 x 28.35 mm
Sensor illumination side	Back side illumination
ADC resolution	8, 10, 12 or 14 bit
Outputs, LVDS	4 data + 2 sync
Setup can control bus	SPI
Clocks	Two external (4MHz & 130MHz) or internal through PLL
Power Supplies	3.3V and 1.8V
Operating mode	Rolling shutter, Global shutter & global shutter with DDS

The CIS120 architecture is also shown in Figure 1 where a column parallel ADC is used to quantise each row of pixels in turn and is controlled by its own readout sequencer which also controls four low-voltage differential signalling (LVDS) channels output the image data and two LVDS synchronisation channels to allow accurate data sampling.

All configuration settings are programmed over a Serial Peripheral Interface (SPI). This includes shutter mode, ADC resolution from 8 to 14 bits and bias current values. An on chip programmable Phase-lock-loop (PLL) can be used to generate the high frequency clocks for the ADC and data output. Pixel timing set by an on-chip sequencer to simplify use and to reduce pin count.

The array row access is separated into two halves (left and right) to allow a wider range of ROI operation.

Teledyne e2v has developed two different chip variants, Capella^{LN} and Capella^{LS}, which are currently being characterised. The Capella^{LN}, Low Noise, is aimed for low noise applications with a full well capacity is limited to approximately 45ke$^-$. The Capella^{LS}, Large Signal, is a modified version where the capacitance of the pixels sense node has been increased allowing the reaching a full well cavity of approximately 80ke$^-$. This is obviously at the cost of an increase of noise in electron.

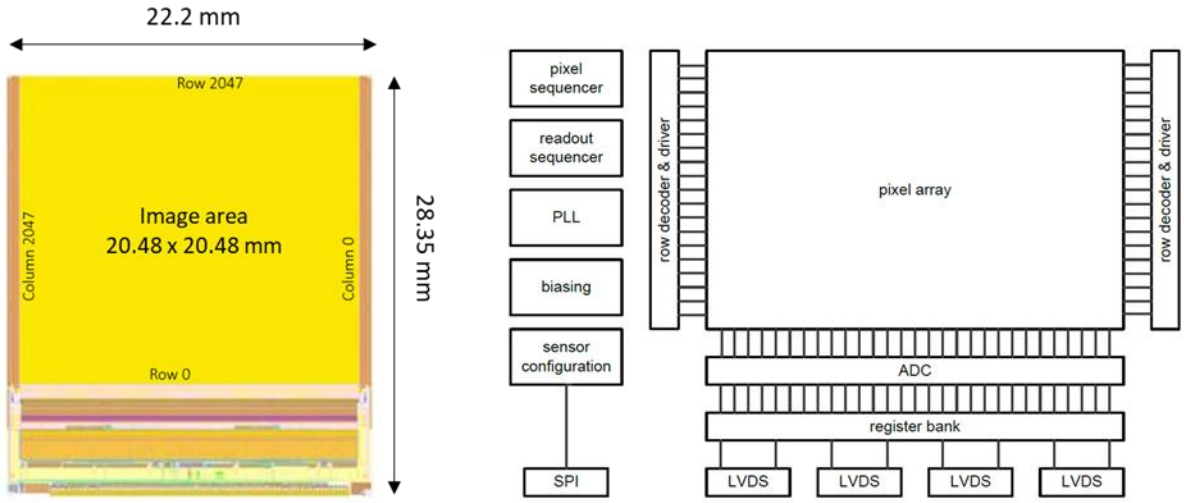


Figure 1 Capella CIS120 Floorplan and block diagram

CIS120 uses a 5T pixel (with a pinned photodiode) that allows Rolling shutter and Global shutter operation mode, Figure 2. It also allows correlated double sampling (CDS) with a rolling shutter to minimised readout noise. The readout path based on a column parallel ADC architecture with a resolution programmable from 8 bits to up to 14 bits

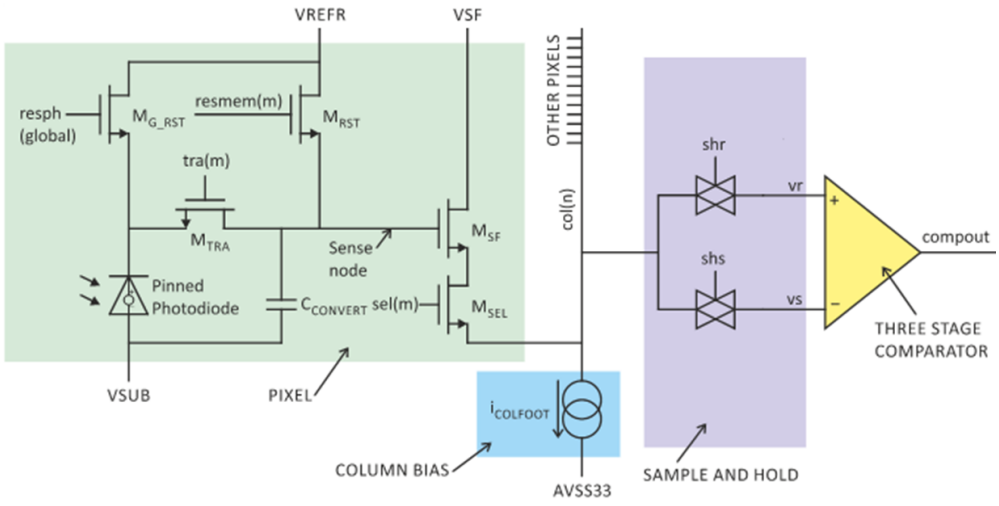


Figure 2. Pixel and simplified sample and hold circuit

3. OPERATING MODES - APPLICATIONS

The CIS120 has been demonstrated to be able to read in any one of three modes (See illustration Figure 3):

- Rolling shutter mode with on-chip analogue CDS for reduce noise at high frame rate
- Simple Global shutter mode, without CDS for high frame rate but at the cost of high noise.
- Global shutter mode with digital double sampling to give most of the benefit of CDS although at the cost of a reduction of the frame rate.

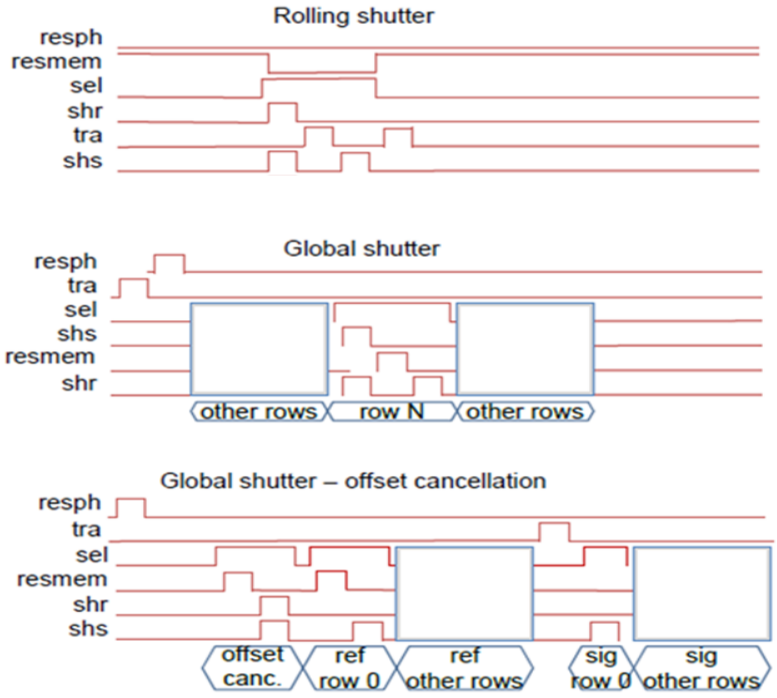


Figure 3. Simplified view of signal involved on the different operating modes that can be implemented (left) and Pixel and simplified sample and hold circuit (right)

In order to achieve the highest possible frame rate the CIS120 operate in pipeline operation, Figure 4 , where the pixel access and AD conversion of each line runs concurrently with the read-out of the previous line, and with the SPI settings (sensor settings & address) for the following line. Each LVDS data output is clocked at 130 MHz in double data rate mode, giving 260 Mbps.

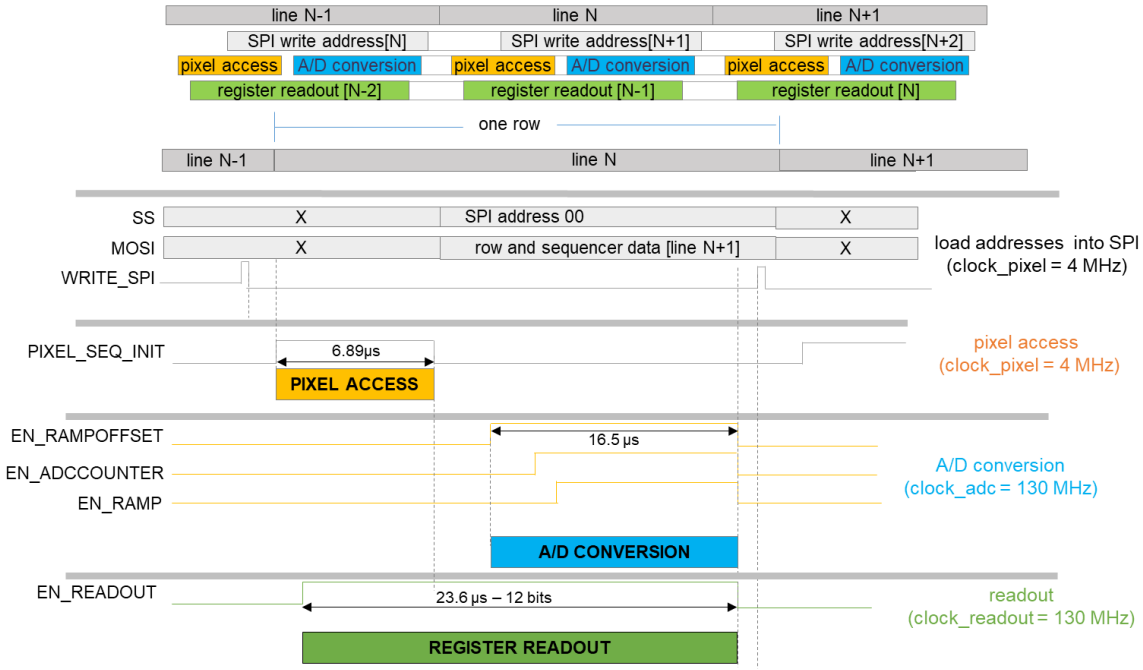


Figure 4. Example of timing diagram for rolling shutter 12 bit – pipeline operation

The different operating modes together with windowing operation allows CIS120 to be used for multiple applications;

- Full frame mode for hyperspectral applications or area imaging.
- Multi-ROI with independent left and right pixel array for star tracker.
- Run very flexibly in multi-linear mode with the possibility of different integration per row.

3.1 Frame rate

The frame rate is largely set by the chosen resolution (8 to 14 bits), the shutter mode and how many rows are to be read (windowing). Table 2 lists the maximum frame rates for whole array readout in rolling shutter mode at each resolution.

Table 2. Maximum rolling shutter frame rates for each resolution

ADC resolution:	8	10	12	14	bits
Pixel access time	8.5	8.5	8.5	8.5	µs
ADC conversion time	1.0	3.9	15.8	63.0	µs
Access + conversion times	9.5	12.4	24.3	71.5	µs
Readout time, 4 ports @260 Mbps	15.8	19.7	23.6	27.6	µs
Time per row	15.8	19.7	24.3	71.5	µs
Time per 2048 rows	32.4	40.3	49.8	146.4	ms
Frame rate	30.9	24.8	20.1	6.8	fps

Using windowing operation, with fewer rows readout (time per row * number of rows), can give much higher frame rates, while the readout for GS in DDS mode will give a lower frame rate, often little more than half the rolling shutter frame rate.

3.2 Relation between integration time and frame rate

The CIS120 uses the external signal PIXEL_SEQ_INIT to drive the pixel sequencer and starts the pixel read sequencer as shown in Figure 4. Integration on each line starts when PIXEL_SEQ_INIT pulse goes down. Integration on each line continue while other lines are addressed and only stops when the line is addressed again on the following frame. Therefore, using the default setting the integration time on each line is equivalent to the max frame time.

Further, there are multiple applications such astronomy where long integration times are required. It is relatively simple to set integration times longer that the default max frame rate by adding delays which can be introduced in different ways such as for example introducing a delay between the ADC of one line and the pixel access of the following line as shown below (Figure 5) or introducing a fix delay between the end of the last line readout and before addressing the first line of the next frame as shown in the next slide. Another option would be to reduce the clocks frequency. By default pixel clock is 4MHz and ADC and readout clocks are both 130MHz but they can be reduced individually.

There are other applications where it is required very small integration times, shorter than the one defined by the default maximum frame rate. In this case, the CIS120 can be configured so the integration time on a row can be reduced by re-setting it during pixel access of a different row.

The idea is to extend the signal PIXEL_SEQ_INIT and while is held high access by SPI to any other different row. by keeping PIXEL_SEQ_INIT high longer the pixel is held in reset mode preventing any light integration which means that any row that is accessed during this period will be re-set and will start integration short after PIXEL_SEQ_INIT goes down again .

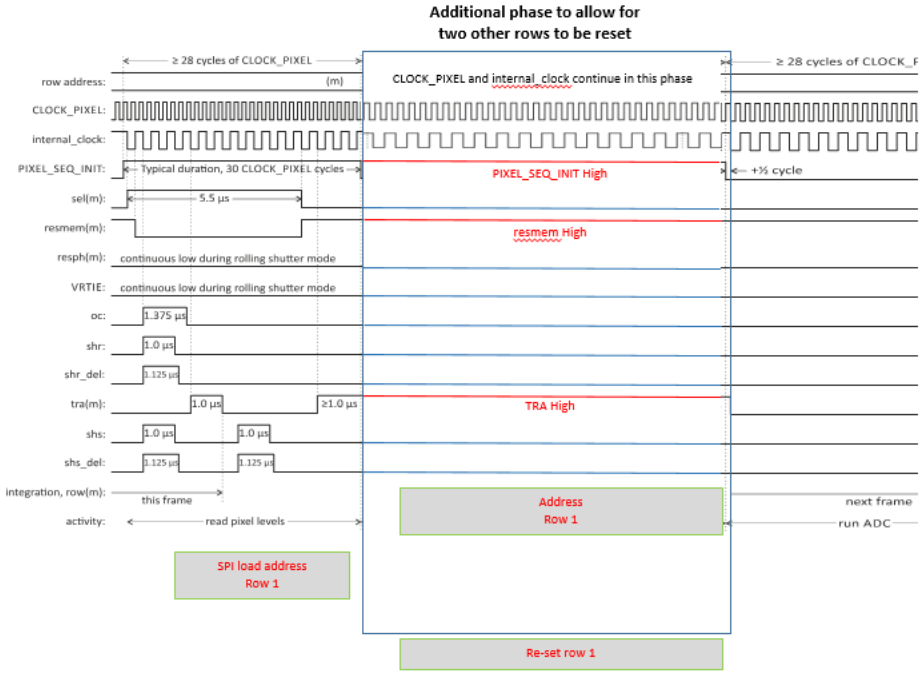
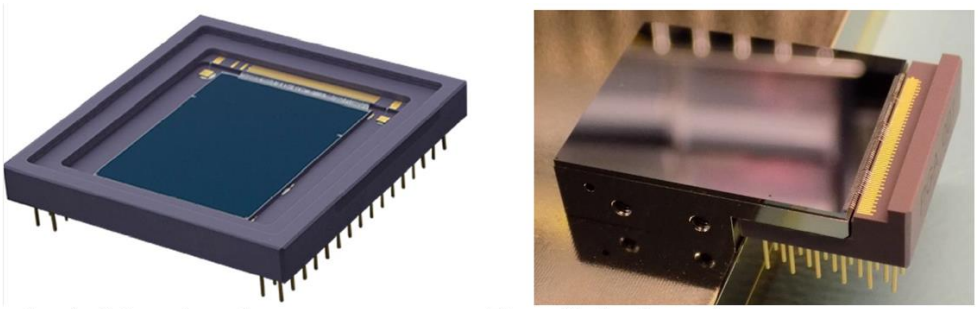


Figure 5. Achieving short integration time by re-setting rows.

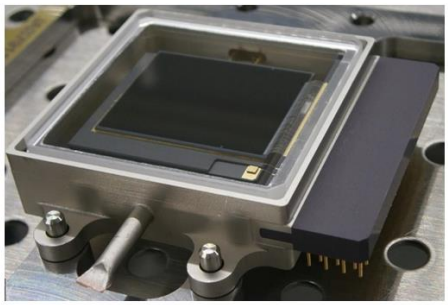
4. DIFFERENT PACKAGES VARIANTS

Teledyne e2v have developed a ceramic PGA (Standard ceramic package) that can currently be ordered for customer evaluation to be used as a baseline for CIS120. A metal and ceramic three-side butting designs have also been developed for use in mosaic focal plane and a sealed Peltier package is also being recently developed.



Standard Ceramic package

Three-side butting package



Sealed Peltier package

Figure 6. Different package options for Capella CIS120

The sealed Peltier package has recently being validated to be used for space applications by going through different environmental test such as Thermal cycling, shock and vibration test. The Standard Ceramic package, which is planned to be used for the Copernicus program, is planning to go through a thorough validation within the next few months.

The three side buttable package has been developed for ground base applications although with some minor modifications could be compatible with space application. It is form by a metal base where the die is attached and wirebond to a ceramic with pin grid arrays which is glued to the metal base.

5. CHARACTERISATION RESULTS

Teledyne e2v has performed extensive characterisation test on early development of CIS120 and also front side illuminated. However, more recently we have completed the manufactured and assembly of the first back side illuminated samples. In this section we present the characterisation results obtained mainly one of the first Capella^{LS} devices, available, from the first wafer, #1, backthinned, tested in rolling shutter 12 bit mode and global shutter in 10 bit mode at -23˚C, except dark signal which was tested at ambient temperature.

5.1 ETF

The electrical transfer function (ETF) is characterised by measuring the output in counts generated by inputting a known difference in electrical signal between the reference and signal levels. The ETF pixel timing is used for this test, so that no optical signal contributes to the measurements. The VREFR supply is clocked between 2 different levels with a signal that is synchronised to when the reference (shr) and signal (shs) are sampled. This enables a known voltage difference to be applied between reference and signal. The output is measured for different signal levels to form the ETF characteristic as shown in Figure 4. ETF measured for four different ADC Ramps (gain 1 to 4) which are configurable by SPI. The designation of gain 1-4 is arbitrary and for reference only.

Gain 4 defines the default ADC ramp slope used for 12 bit operating mode as allows the sensor to saturate close to the ADC count saturation providing an optimum match between pixel range and ADC input range. Gain 2 defines the default ADC ramp slope for 14 bit operation which allows lowering the LSB below the expected readout noise so that can be measure it. Therefore, it is also used to measure the noise in any ADC bit mode.

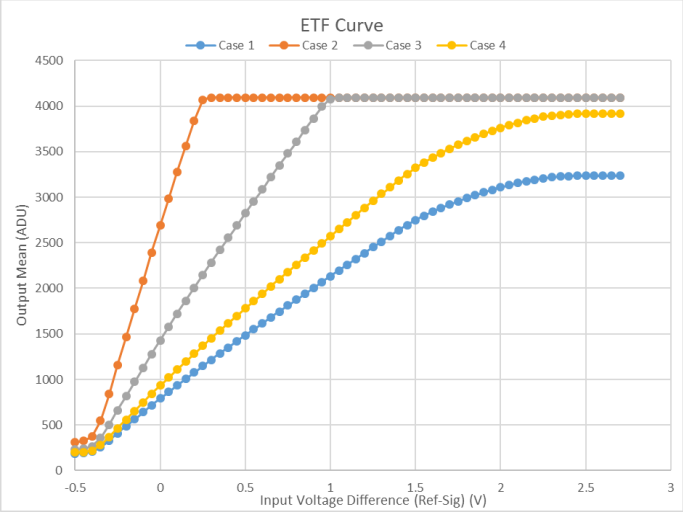


Figure 7. ETF curve for 4 gains (cases) measured on CIS120 for 12 bit mode

5.2 X-Ray CCF

An iron-55 (Fe55) low level X-ray source is used during image acquisition to provide a known signal level in the pixels and the Charge to Code Factor (CCF) is the conversion gain (in ADU/e^-) from electrons collected by the photodiode to the output of the device. Due to the sparse nature of the x-ray events it is only possible to calculate the CCF as an average of every pixel, not on a pixel by pixel basis. Figure 8 shows the CCF measured in rolling shutter for 12 bit (which is the default operating mode) and similar plots would be expected in global shutter 12 bit simple mode. However, a discrepancy is observed which is attributed to the fact that global shutter simple mode is measured at 10 bit ADC resolution, which is the operating mode required for the Copernicus CO2M mission.

Table 3 - X-Ray CCF Results

	Rolling Shutter 12 bit	Global shutter 10 bit	Units
X Ray CCF – Gain 4	0.0384	0.0096	ADU/e-
X Ray CCF – Gain 2	0.1307	0.1291	ADU/e-

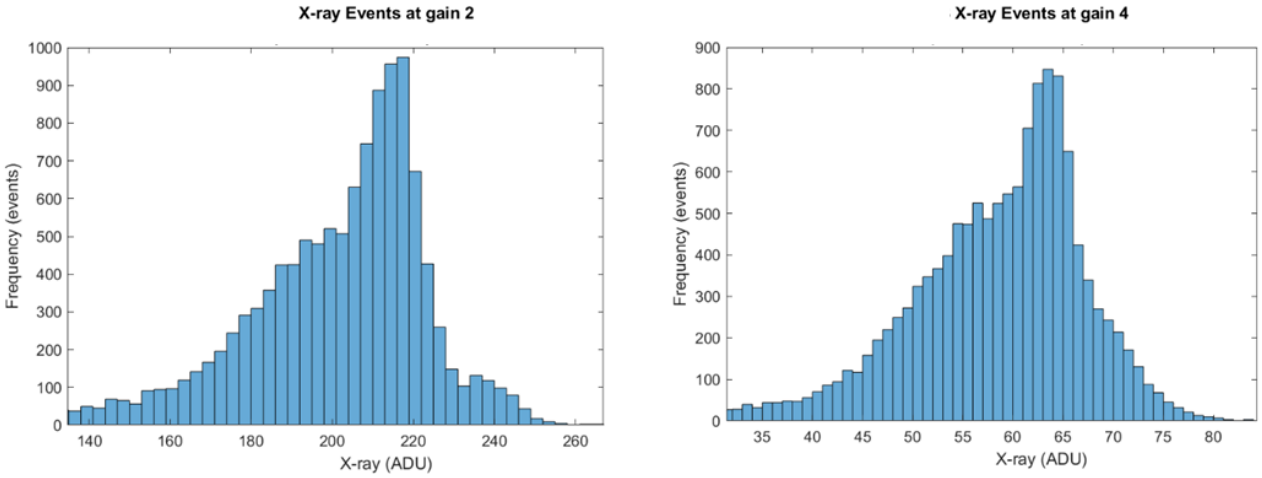


Figure 8. X-Ray CCF histogram in Rolling shutter mode for gain 2 (left) and gain 4 (right)

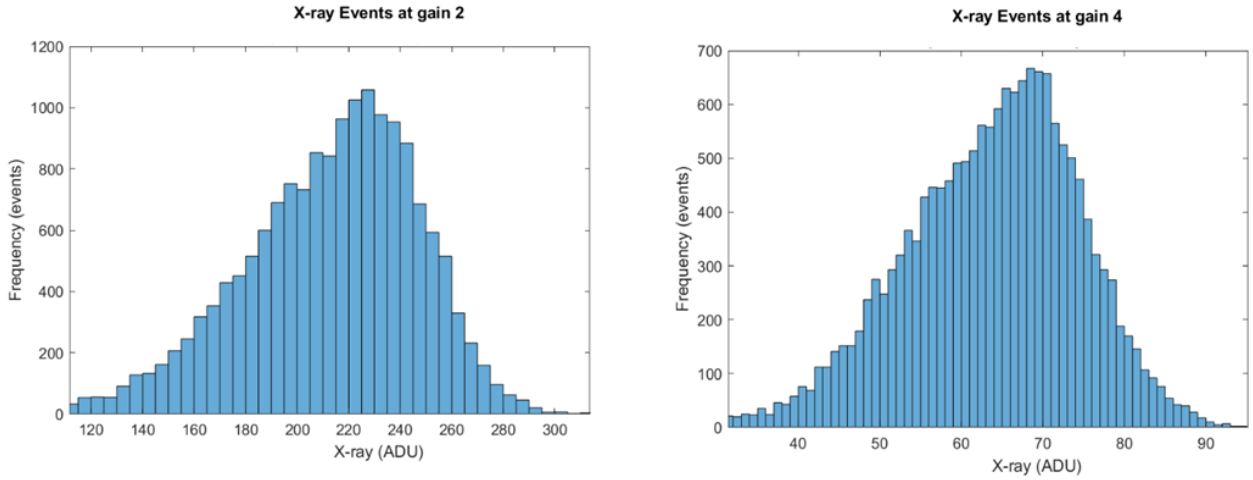


Figure 9. X-Ray CCF histogram in Global shutter mode for gain 2 (left) and gain 4 (right)

5.3 Noise

The rolling shutter noise results are close to the expected value. The global shutter simple mode (without DDS) noise is as expected considerably higher than in rolling shutter results since CDS is not implemented and therefore the KTC noise cannot be removed.

Table 4 – Noise results

	Rolling Shutter	Global shutter	Units
Readout Noise (gain 2)	9.30	60.04	e- rms
Readout Noise (gain 4)	13.49	82.06	e- rms

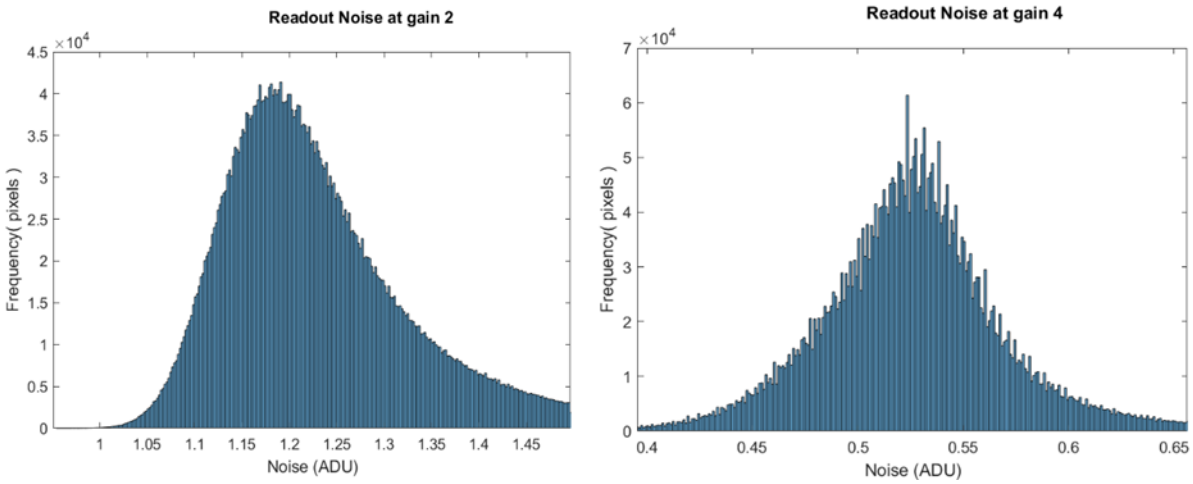


Figure 10 - Rolling shutter noise histogram for gain 2 with CCF=0.1307ADU/e- and gain 4 with CCF=0.0384

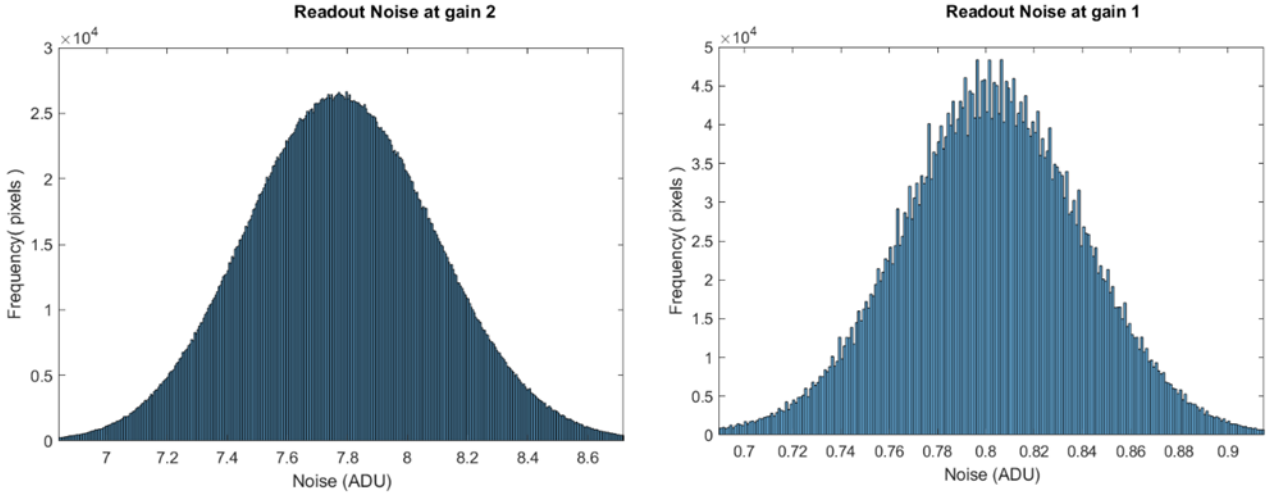


Figure 11 Global shutter noise histogram for gain 2 with CCF=0.1291ADU/e- and gain 4 with CCF=0.0096 ADU/e-

5.4 Dark Signal and Dark-signal Non-Uniformity (DSNU)

Due to the very low dark signal value obtained at -23˚C the results from this run of test carried out with the main device from wafer #1 used for this characterisation are not reliable enough. Instead, a set of results from a device from a different wafer #2 previously characterised for dark signal at ambient temperature, 21°C, is presented in this section.

Table 5 shows the dark signal in rolling shutter and global shutter which are within expectation at 21°C. It is important to point out that the global shutter results are significantly higher, 391 e-/pix/s, than in rolling shutter, 44 e-/pix/s. This higher value comes from the timing regime used for resetting the sense node. In rolling shutter mode the sense node is reset just prior to the transfer of charge from the photodiode. In global shutter however the sense node is not cleared before the TRAGL (transfer global) pulse, Figure 12 . This means that the dark signal generated on the photodiode is added to the dark signal generated on the sense node before being measured. Because the sense node is unpinned the dark signal rate is around 3 times higher. However, this is not a significant issue on applications where integration time is short.

Table 5 - Dark signal results

	Rolling Shutter	**Global shutter**	**Units**
Dark Signal	44	391	e^-/pix/s

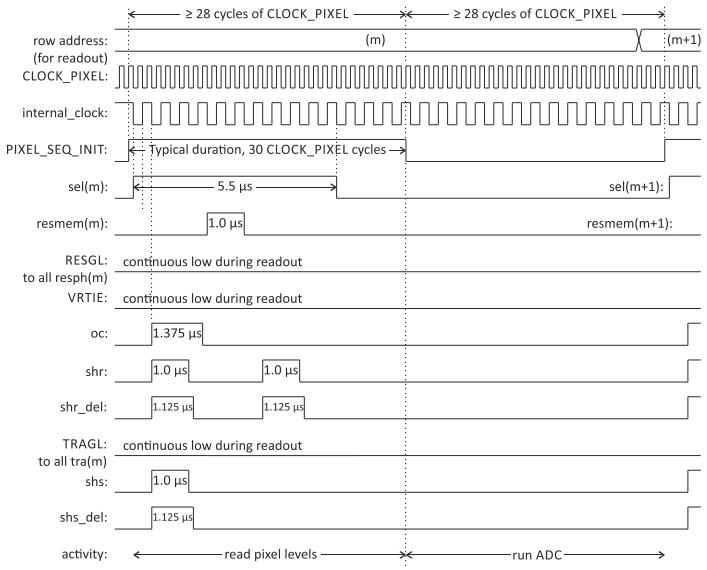


Figure 12. Pixel sequencer timing for single global shutter. You can see that Resmem(m) is only pulsed prior to reading the reference and not the signal.

For applications where it is required to achieve low dark signal in simple global shutter mode there is the possibility of resetting the sense node prior to the TRAGL, as proven in Figure 13 where it has been measured a dark signal of 47 e^- /pix/s, in line with rolling shutter mode. However, since the pulse for resetting the sense nodes is created by the internal pixel sequencer, there will be an impact on the frame rate as the external signal required to be used will affect other internal signals.

.

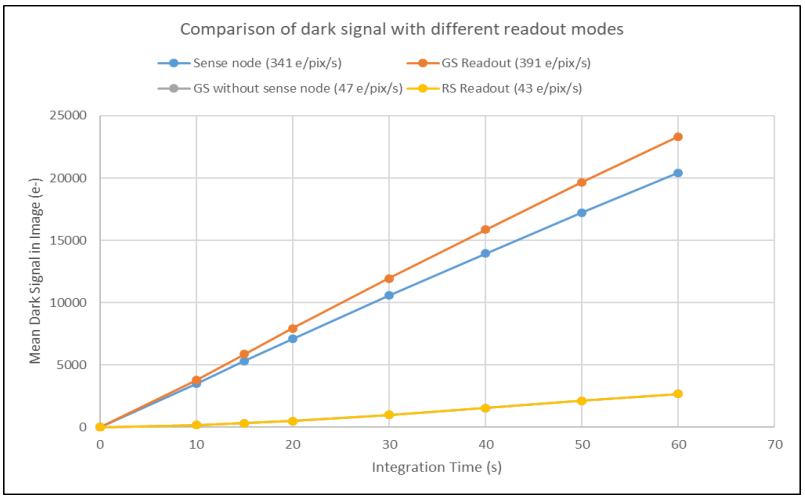


Figure 13. Dark signal results for Global shutter and Rolling shutter. Also included are results from global shutter while not transferring charge to the sense node and without transferring charge from the photodiode

The DSNU of rolling shutter mode is in line with expectation at 34 e^-/pix/s. the higher dark signal in global shutter mode means that the DSNU is also higher. In rolling shutter mode there is no identifiable DSNU pattern in the images. In global shutter mode there is a slight ramp up the image caused by charge still being generated at a fast rate on the sense node while the device is being read out. Row 2048 will have longer to generate this charge than row 0 (see Figure 14 and Figure 15).

Table 6 – DSNU results

	Rolling Shutter	**Global shutter**	**Units**
DSNU	34.3	171.5	e-/pix/s

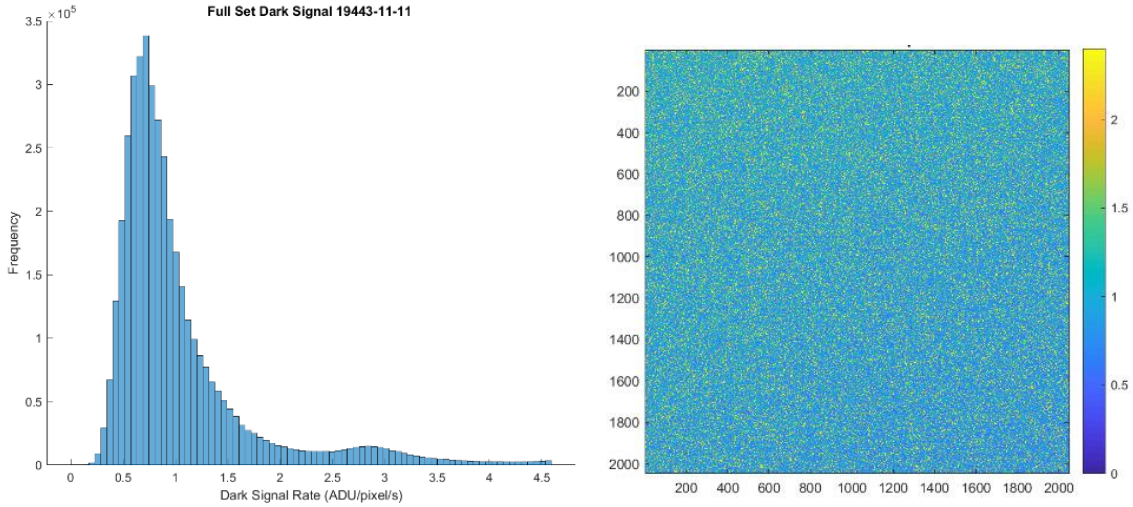


Figure 14 - Rolling shutter dark signal histogram.

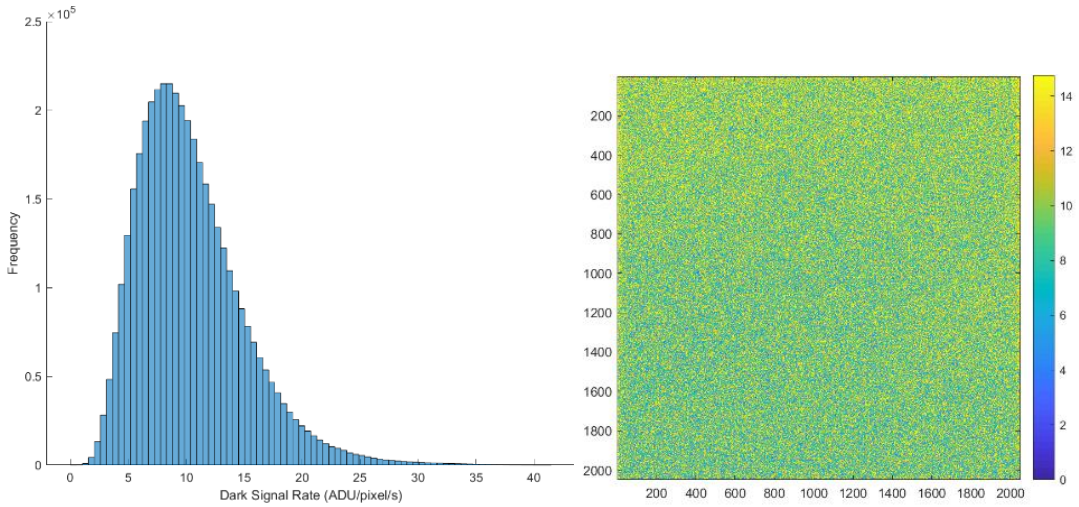


Figure 15 – Global shutter dark signal histogram.

5.5 Saturation level (Qsat), Linear saturation level (Qlin) and Non-linearity

The Qsat obtained in global shutter and rolling shutter are very similar as expected with a difference of global shutter less than 1ke$^-$.

QLin is defined here at the point where the non-linearity exceeds 10%. The Qlin value is expected to be below that of Qsat and in general results are in line with expectation. The median device Qlin results, after optimisation, are slightly higher in rolling shutter mode than global shutter mode but only by around 1.2ke$^-$. The non-linearity results are calculated as the maximum linearity error of a pixel over the range 5% to 95% of the calculated Qlin value.

During the bias optimization it has been found that the device requires to be operated with different biases in global shutter mode with respect to rolling shutter mode in order to maximise Qsat and Qlin. VREFR has to be increase from 2.9V to 3.1V and VHIGH from 2.80 V to 2.95V.

Table 7 – Qsat, Qlin and Non-lin results

	Rolling Shutter	**Global shutter**	**Units**
Qsat	72,200	71,127	e$^-$/pix
Qlin	69,680	68,446	e$^-$/pix
Non-lin	2.40	2.02	%

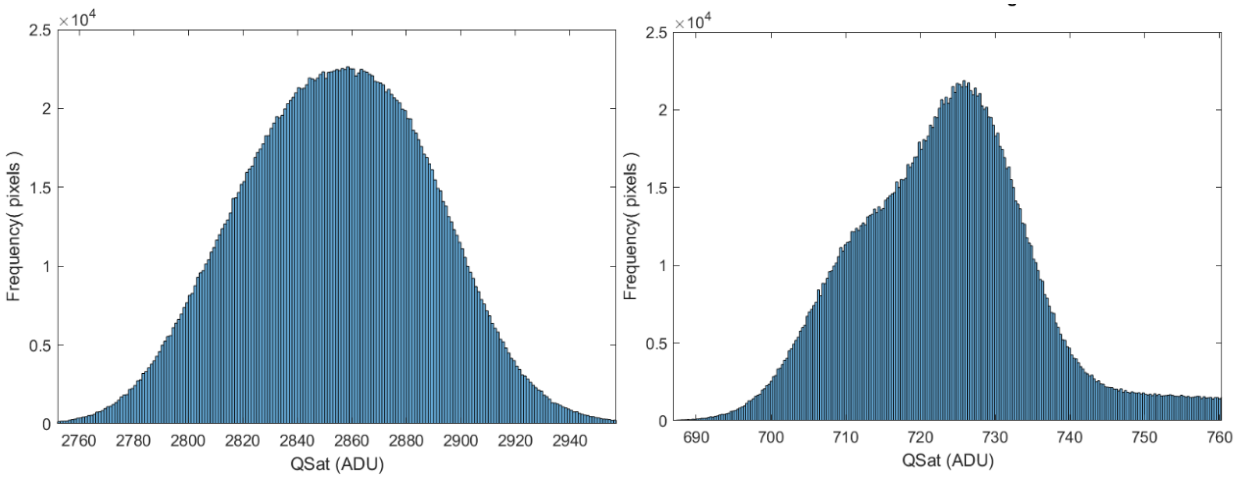


Figure 16 - Rolling shutter (left) and Global shutter (right) Qsat maps.

5.6 Lag

Table 8 shows the lag results at three different signal levels. The lag results are around the expected values for rolling and global shutter, less than 1%, with global shutter experiencing more Lag. It was found during the optimisation of Qlin described in section 5.5 that the increase of VREFR and VHIGH also helped improve the global shutter lag.

Table 8 - Lag results

	Rolling Shutter	Global shutter	Units
Lag at 1ke-	0.070	0.209	%
Lag at 20ke-	0.012	0.220	%
Lag at 60ke-	0.017	0.156	%

5.7 QE

Preliminary QE measurements have been carried out on the devices. As can be seen the QE measured follows quite well the profile of the predicted QE although it is slightly lower. At this stage, it is not clear if this discrepancy is due to a backthinning process variability or to the calibration of the camera.

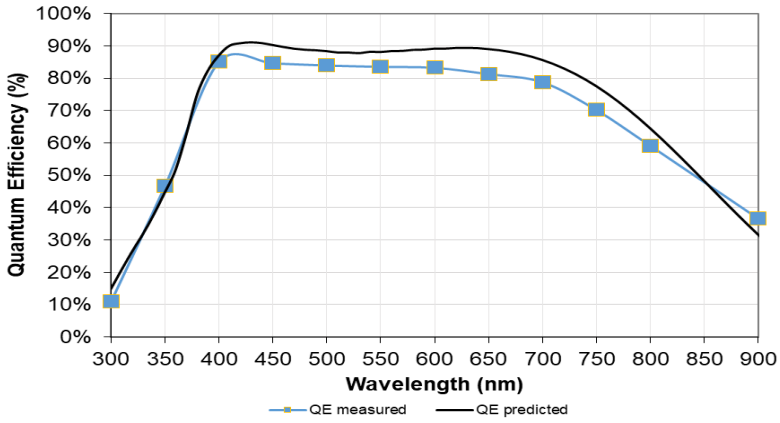


Figure 17. QE predicted and QE measured on a back illuminated CIS120 device.

5.8 Summary EO results

Table 9 summarises the EO results presented in the previous sections from device from wafer #1 in RS 12 bit mode and simple GS in 10 bit mode at -23ºC, except dark signal and DSNU, tested at 20ºC on a different characterization device, from wafer #2.

Table 9. Summary EO results.

Parameter	Results		Units
Operating Mode	RS	Simple GS	
ADC resolution	12	10	Bits
CCF Xray - Gain 4	0.0384	0.0096	(ADU/e-)
CCF Xray – Gain 2	0.1307	0.1291	(ADU/e-)
Readout Noise – Gain 4	13.49	82.06	e- rms
Readout Noise – Gain 2	9.30	60.04	e- rms
Qsat	72200	71127	e-
Qlin	69680	68446	e-
Non-Lin	2.40	2.02	%
Dark Signal	44	391	(e-/Pix/s)
DSNU	34.3	171.5	(e-/Pix/s)
Lag at 1ke- signal level	0.070	0.209	%
Lag at 20ke- signal level	0.012	0.220	%
Lag at 60ke- signal level	0.017	0.156	%

6. TRL6 ACTIVITIES

CIS120 devices are going through different radiation and environmental campaigns to increase the TRL of the sensor. Two devices have now completed heavy Ion test in order to evaluate latch up and SEL and another two have also completed proton irradiation. Two additional devices are waiting to go through gamma radiation within the next few weeks so it is expected to be completed by April 2021.

6.1 Proton Irradiation

Two devices underwent proton irradiation of $5x10^{10}p/cm^2$ and as expected the main difference is in dark signal. Results shows an increase in dark signal of approximately 45 times which match relatively well with heritage.

Dark signal without the contribution from the sense node has also been investigated and shows that at post irradiation the increase in dark signal is approximately 7 times lower than with the sense node which is in line with the results obtained with other Teledyne e2v CMOS sensors on previous programs.

A small increase in x-ray CCF and similar reduction in QSat has also been observed but we are carrying out further investigation into whether extra hot pixels are having effect on x-ray. Post irradiation histogram shows an extended tail of hot defects

Table 10. Pre and post proton radiation EO results obtained in simple GS at -23ºC from device #3.

Parameter	Pre radiation	Post proton Rad	Units
CCF Xray Gain 4	0.0098	0.0103	(ADU/e-)
CCF Xray Gain 2	0.1342	0.1389	(ADU/e-)
Readout Noise– Gain 4	79.67	76.70	e- rms
Readout Noise - Gain 2	59.01	57.54	e- rms
Qsat	69721	67037	e-
Qlin	68255	64444	e-
Non-Lin	2.21	1.95	%
Dark Signal	0.34	15.32	(e-/Pix/s)
DSNU	3.85	29.50	(e-/Pix/s)
Dark Signal SN	0.01	2.21	(e-/Pix/s)
DSNU SN	0.68	21.03	(e-/Pix/s)
Lag at 1ke-	0.355	0.293	%
Lag at 20ke-	0.337	0.306	%
Lag at 60ke-	0.192	0.251	%

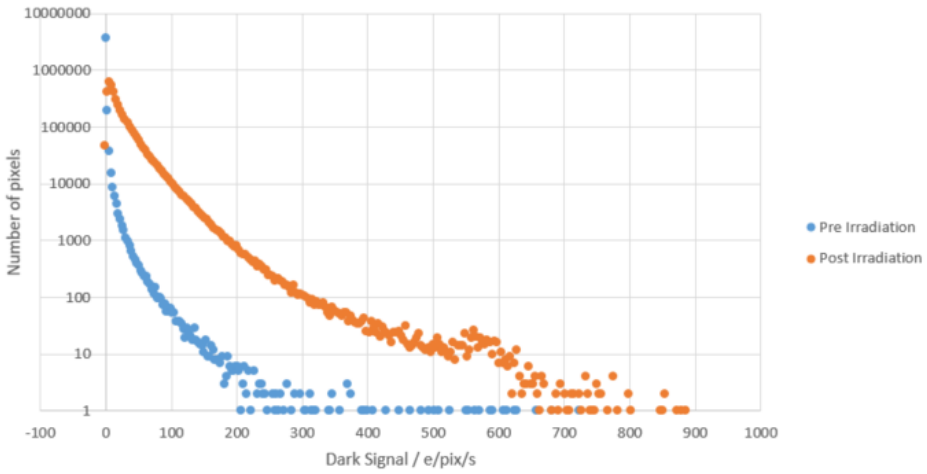


Figure 18. Dark signal pixels distribution pre and post irradiation

6.2 Heavy Ion test

Heavy Ion test has been performed to investigate the susceptibility of the CIS120 to latchup and Single Event Upset (SEU). As shown in Table 11, two devices were tested up to 62.5 MeV·cm²/mg LET.

In order to detect latchup all the sensor biases were monitored and the compliance limit set to around 10 times. No latch-up were detected on any of the two devices up to 62.5 MeV·cm²/mg LET. During all irradiations, the devices continued imaging correctly implying also no obvious signs of SEU neither up to 62.5 MeV·cm²/mg LET. The devices were also tested with and without the PLL and no difference was detected. Therefore, it can be concluded that the PLL is also immune to latch-up and SEU up to 62.5 MeV·cm²/mg LET.

Table 11. Different Heavy Ion test runs performed on two devices.

Device	PLL used	LET (MeV/cm^2.mg)	Flux (ions/cm^2/s)	Fluence (ions/cm^2)
Device #5	No	62.5	1x10^4	1x10^7
	Yes	62.5	1x10^4	1x10^7
Device #6	No	32	1x10^4	1x10^6
	Yes	32	1x10^4	1x10^6
	No	52	1x10^4	1x10^6
	Yes	52	1x10^4	1x10^6
	No	62.5	1x10^3	1x10^7
	Yes	62.5	1x10^3	1x10^7

After these harsh test was performed, two usual changes were observed; An increase in dark signal over 100 times, which is expected due to the large ionising doses induced by the heavy Ion radiation. An increase of noise was also observed which can be explained due to the increase in dark signal shot noise.

7. CIS220 VARIANT - HIRHO TECNOLOGY FOR NIR APPLICATIONS

Teledyne e2v is working with Open University and ESA on the development of the HiRho technology for Capella, CIS220, which is based on High-resistivity and very thick epitaxial silicon which enables full depletion for thick material giving very good MTF and high QE at long wavelengths (NIR) [2].

.

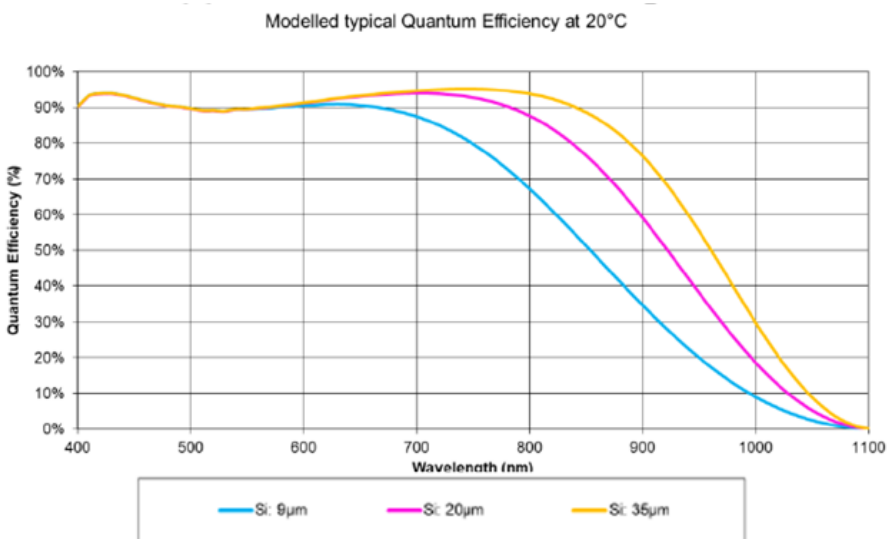
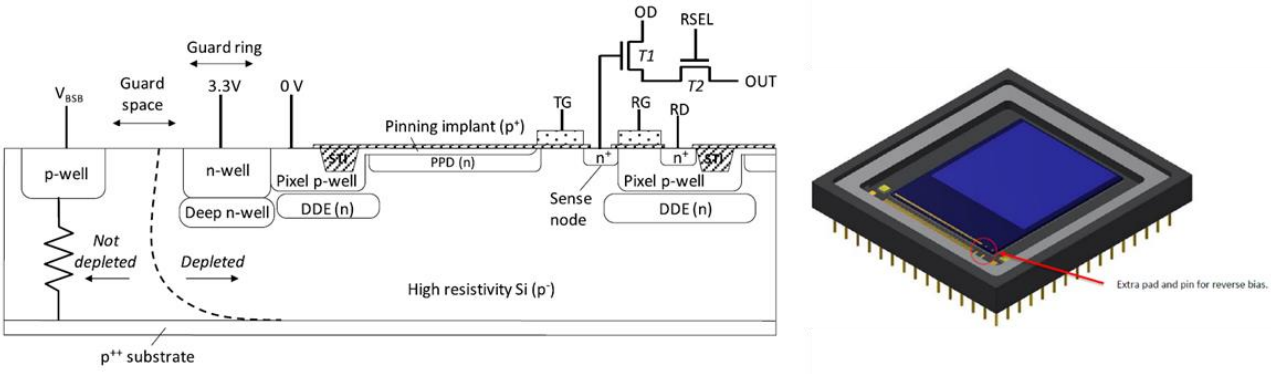


Figure 19. QE predicted for different silicon EPI thickness. NIR applications

A primary feature includes back substrate bias voltage to ensure full depletion of the thick silicon. Additional special design features have been included that enable high gate to substrate potentials to be applied without current leakage between back and front substrate connections

CIS120 is being used as the baseline to validated HiRho technology. This reduces the risk associated with a new design as the changes are only around the layout and implant modification. Compatible with standard ceramic package where extra bond pad for back-bias voltage was already taken into account, Figure 20.



[3]

Figure 20. Cross section diagram of the fully depleted PPD pixel design (left) and CIS120 on standard ceramic package showing back bias connection (right).

.

One of the risks with supplying a reverse or back bias (BB) is this could create leakage paths that would catastrophically damage the sensor. To prevent this, a specific implant is required (known as the Deep Depletion Extension (DDE) implant). For the CIS220 front face characterisation Teledyne e2v has evaluated 6 variants with three different implants and thicknesses of 25 and 40 µm.

The first front face samples have been assembled and characterised and the preliminary results show that for implant energy 1, leakage occurs at a very low value for both 25µm and 40µm thick device. Therefore, it is unlikely this implant energy will be selected. However, for implant energy 2 and 3 both show increased back bias voltages is achievable. These results are in line with the TCAD simulations done prior to manufacturing.

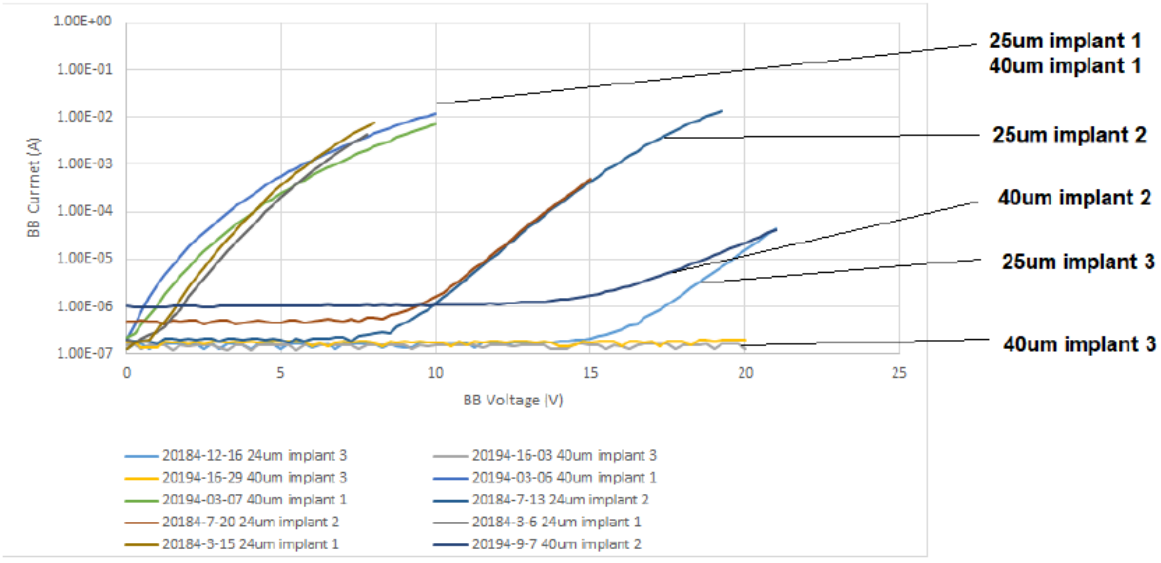


Figure 21. Back bias leakage measured for different implants

For the 40µm implant energy 3, no leakage was observed up to a BB = -20V. A measurement in dark and with signal was also checked and show that the device still functioned up to a back bias of -25V. Figure 22 shows Images taken with a pattern on top of the sensor at different back bias voltages. On the image with no applied back bias there is no structure observed in the image and this is as expected as there is a very small depletion depth. Therefore, charge generated in the silicon will diffuse and be collected at different pixels than where they were generated. As back bias is increased the depletion depth increases and the structure starts to appear more clear. At BB = -20 it would be expected it is expected the depletion depth to be close to full depletion as it appears that most of the charge is collected in the pixel in which it was generated.

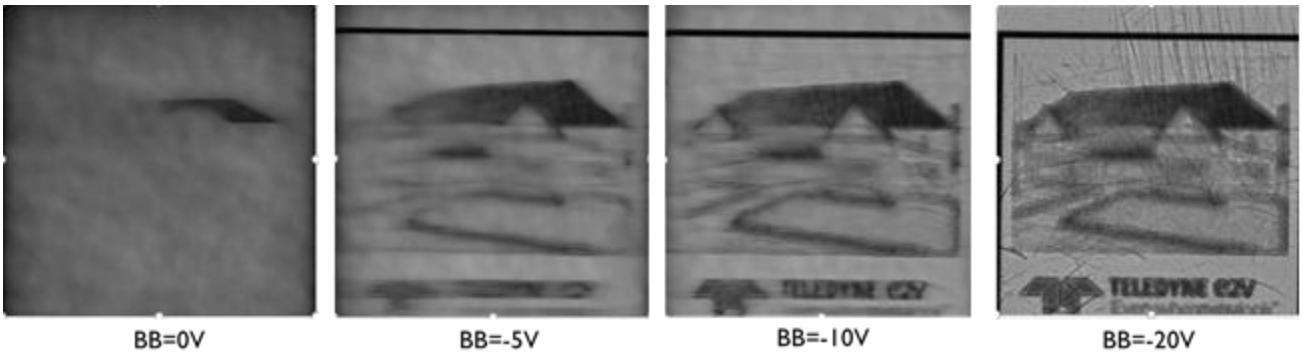


Figure 22. 40µm thick implant energy 3 device. Images taken at different back bias voltages

Currently different variants are being backthinned and first devices are expected to be evaluated in April 2021.

8. CONCLUSION

This paper has presented the die design and different package variant available for the Capella CIS120. It has also shown initial EO results for the variant to be used for the Copernicus CO2M mission together with the validations necessary to reached TRL6. The only activity left is gamma radiation which is planned to be completed in April 2021.

We have also presented a new variant, CIS220, HiRho tecnology for NIR applications, and the preliminary successful front face results. The next phase will consist on testing back side illuminated devices planned also for April 2021.

REFERENCES

[1] Bown. M., "Teledyne Imaging to supply image sensors for new Copernicus Earth observation missions", https://www.teledyne-e2v.com/news/teledyne-imaging-to-supply-image-sensors-for-new-copernicus-earth-observation-missions/ (14 July 2020)

[2] Mark S. Robbins, Pritesh Mistry, and Paul R. Jorden. "Detailed characterisation of a new large area CCD manufactured on high resistivity silicon", Proc. SPIE 7875, Sensors, Cameras, and Systems for Industrial, Scientific, and Consumer Applications XII, 787507 (16 February 2011)

[3] Xiao Meng, Konstantin D. Stefanov , *Member, IEEE*, and Andrew D. Holland. "Proton and Gamma Radiation Effects on a Fully Depleted Pinned Photodiode CMOS Image Sensor", ieee transactions on nuclear science, vol. 67, no. 6, june 2020