Thinking small: challenges for metrology at century's end

William H. Arnold
Advanced Micro Devices,
Technology Development Group
1 AMD Place, MS 78, Sunnyvale, CA 94088

Abstract

This paper will consider the challenges facing linewidth metrology as devices shrink to the 100nm level and below, forcing all of us to "think small". Significant improvements are needed in low voltage SEM resolution and measurement reproducibility. The applications of electrical probe metrology should be expanded through clever construction of test devices. Atomic force microscopy offers a novel way to measure feature size, as well as wall profiles and material thicknesses, but suffers from slow scan rates and data acquisition cycles. Advances in AFM need to address more rapid CD measurements and real-time imaging.

Feynman's challenge

In a talk delivered to the annual meeting of the American Physical Society in late 1959 (1), the famous physicist Richard Feynman challenged the science and engineering community to explore the universe of the microscopic, to build tools and machines that could operate at smaller scales, to see that "there is plenty of room at the bottom". He outlined the logic behind the basic truism of the modern electronics industry, that smaller computers could be both more powerful and more efficient, simultaneously. He offered $1000 to the first person who could demonstrate the ability to write the contents of the Encyclopedia Britannica on the head of a pin. This is equivalent to a reduction of 25,000X, or in lithographer's terms, 10 nm L/S. Feynman speculated that a scanning electron microscope could be modified to write such small features. The prize was not claimed until 1987, nearly 30 years later, when T. Newman (then at Stanford) wrote the first page of **A Tale of Two Cities** at 25,000X reduction, using, as forecast by Feynman, a beam of electrons to write the passage in resist. This level of lithography, while feasible, is not expected to be used in volume IC production until 2027, at the current rate of progress, as dictated by Moore's Law. See Figure 1.

In his talk, Feynman also challenged the community to improve the resolution of the electron microscope by 100X.At that time to the best resolution demonstrated was about 1nm. Transmission electron microscopes have improved perhaps ten-fold in resolving power since then (2), and low voltage scanning electron microscopes commonly used in the fab for measurement and inspection have improved from about 20nm in the mid 80s to 5nm or less today (3). See Figure 2. Yet, even with all this progress, think what an improvement a further five-fold increase in image resolution, to 1nm on low voltage SEMs, would bring to both inspection capability and measurement reproducibility!

0227-786X/97/$10.00

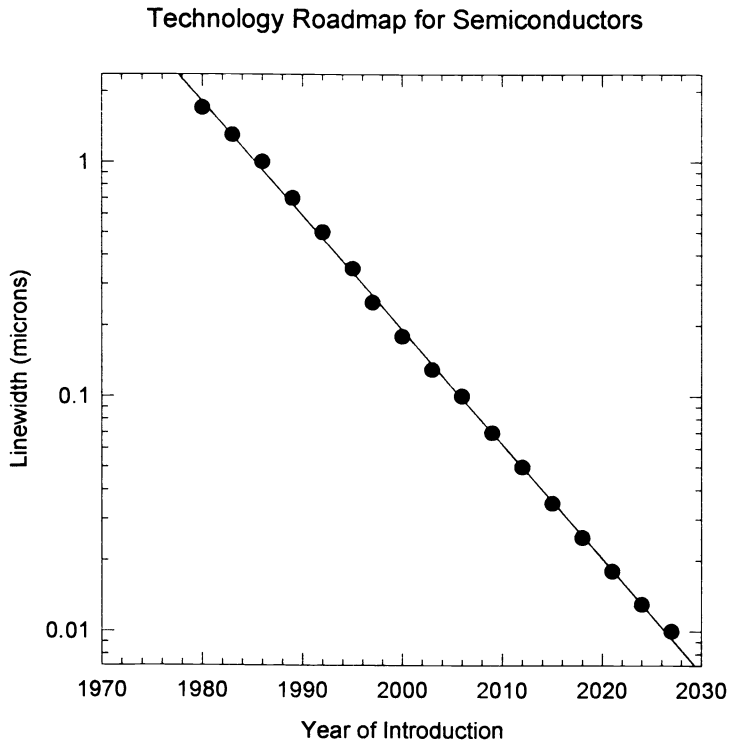

Figure 1. IC requirements : minimum feature size versus time. The Feynman resolution is 0.01 micron = 10 nm L/S. The industry is currently (1997) putting 250 nm lithography into production.

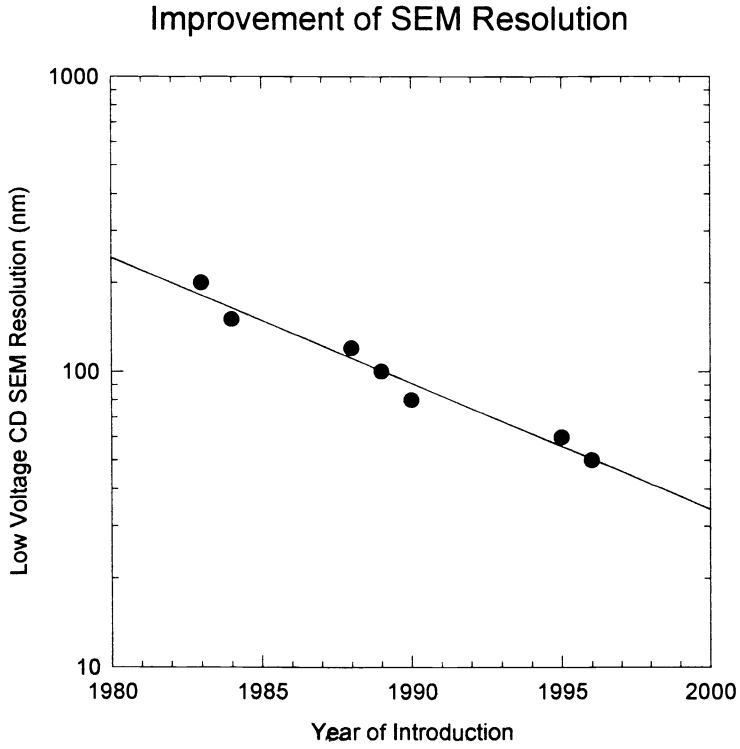

Figure 2. Low voltage SEM resolution versus time.

As surreal as it seems, this is the level of measurement precision and repeatability that will be required by the integrated circuit industry for the production of the next century's high speed microprocessors, communications devices, and multi-gigabit memories. Because metrologists work at a level 10 to 100X smaller than the lithographer, we will have to "think small" first.

Metrology is an enabling technology for lithography

In order to meet the increased worldwide demand for higher performance computation and communications products, the steady reduction of lithographic feature size in IC production has accelerated in recent years and has become a headlong rush. A good example is the rapid reduction in gate length of CMOS logic devices, needed to drive the increased performance of microprocessors. In many cases the lateral scaling of dimensions has not been accompanied by a similar scaling in the vertical due to the requirements for interconnect performance and reliability. Thus structures of extraordinary density and relatively high aspect ratio must be inspected and measured. This trend has put strain on IC lithographers, lithographic equipment and material suppliers, mask suppliers, and, not least, on those who attempt to provide metrology solutions.

Why is it so important to improve measurement reproducibility? The chief reason is the key importance of controlling gate length in high speed CMOS transistors (4). Microprocessor speed is one of the most important determinants of the price that an IC maker can get for the part. The microprocessor's speed results from a combination of circuit design and process technology. Of key importance to the process technology are the gate delay, the time it takes a single transistor gate to switch on or off, and the transistor drive current. Both gate delay and drive current are proportional to the inverse of the gate length.The effective gate length is largely determined by lithography and etch (micropatterning) process capability and control. It is not enough to have a short gate length. All gate lengths have to be tightly controlled across the full chip in order that the timing of signals can be well-correlated and placed in sequence.

The challenges for CD metrology are numerous. For gate linewidth, SEM CD metrology needs to provide good correlation with device performance as well as heroic levels of dimensional stability of the order of a few nm. 150 nm gates can be expected in microprocessor production before the end of the century, with 100 nm gates in 2001 or 2002. For spaces, or trenches, and holes, automatic inspection should tell the engineer that the openings are clear and sized properly, with the desired wall angles, even for high aspect ratio openings in dielectrics or silicon. 200 nm contact holes in 1 micron of dielectric can be expected for production before the end of the century.

Overlay budgets will fall to less than 50 nm for device production at the beginning of the new century, placing demands on registration metrology to supply results with better than 10 nm repeatability. A review of the needs for overlay metrology will have to be left to another paper.

Another problem of extreme complexity is the management and analysis of the flood of data from metrological tools, defect monitors, and in situ sensors, in order to control and optimize the total fab process.

Important new technologies have been introduced to the fab in the 1990s to address the measurement and inspection challenges posed by the ever-shrinking transistor. These include automatic low voltage CD SEMs, atomic force microscopes for linewidth measurement and profilometry, spectroscopic ellipsometry for film thickness measurement and the determination of optical properties, and automatic SEM-based defect detection systems. These tools allow the metrologist to probe device structures at an ever-increasingly fine level, and to visualize the atomic nature of films and their interfaces. These tools are also increasingly complex and expensive.

Low Voltage CD SEM

Low voltage scanning electron microscopes were first introduced to the fab for CD metrology at about the 1 micron level (6). Today , low voltage SEMs operating at about 1kV are used routinely to measure critical dimensions at the 250 nm level. At 1kV, an electron has a wavelength of 0.4 A, offering the intriguing possibility of resolving atomic level detail. Unfortunately, this prospect continues to be out of reach, because of limitations imposed by the instrument, by the features on the wafer, and by the nature of the interaction between electron beam and the wafer. Commercial instruments have improved in image quality and resolution from around 20nm at the time of first introduction to the fab area to 5nm or less in today's best tools (3).

The resolution of low voltage scanning electron microscopes is much superior compared to optical microscopes because the operating wavelength is nearly 10,000X smaller. However, the resolution improvement is not 10,000X as the numerical aperture of the SEM is kept relatively low due to the effects of aberrations. Low V SEM resolution is limited chiefly by chromatic aberration, which has not been dealt with effectively as it is in light optics, where matched doublets are formed with glasses of different dispersion properties to cancel much of the color aberration. Could the recent development by Rempfer of an electron "mirror" (containing a hyberbolic electric field) be used in low V SEMs to reduce the effects of chromatic aberration (5)?

In recent years, low voltage SEMs have become almost fully automated, which has improved both the throughput and the measurement repeatability, by eliminating operator to operator variations. Figure 3 shows the improvement of 5-site CD measurement throughput as a function of time for low voltage CD SEMs. On the downside, these instruments are more than a generation behind in their measurement repeatability, as required by the SIA Lithography Roadmap. The cost and complexity of these tools have grown with the amount of automation and degree of image quality and measurement precision required. Figure 4 plots the list price of low voltage CD SEMs as a function of time.

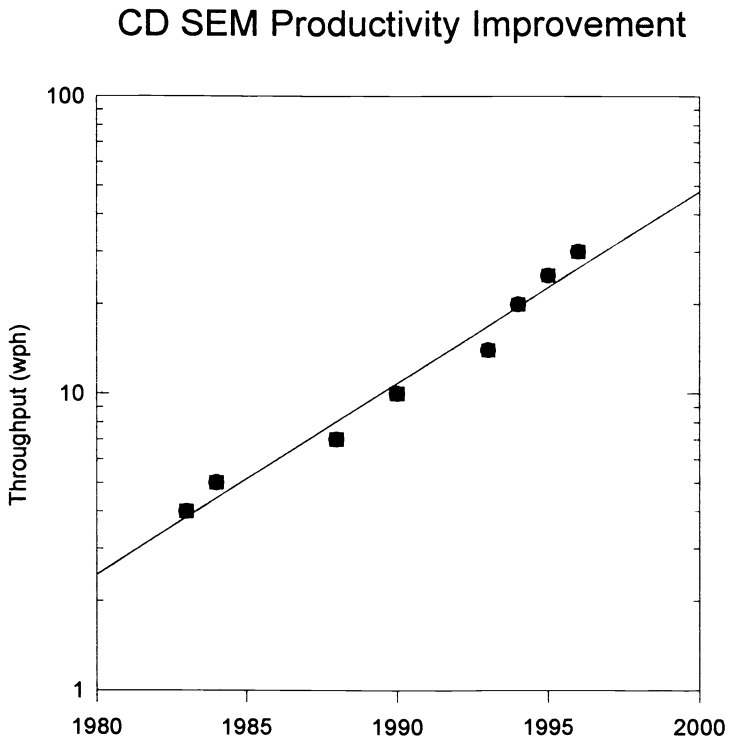

Figure 3. Throughput versus time for 5-site measurements, low voltage CD SEMs.

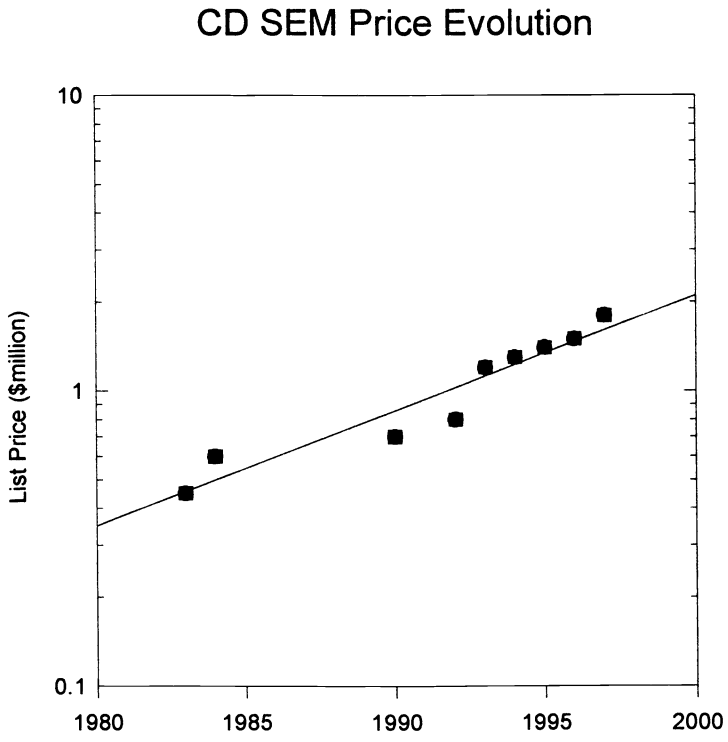

Figure 4. Low voltage SEM list price versus time.

Beyond resolution, there exist other limitations which the metrologist would welcome solutions to. A common problem is the poor imaging of high aspect ratio openings in resist on dielectric surfaces. Nyyssonen has analyzed the reduction in collection efficiency of low voltage SEM detectors as a function of collection field strength and aspect ratio of the features imaged (8). Wafer charging effects and high aspect ratios make it very difficult to collect a usable signal from deep contact holes or spaces in resist. Two methods being employed currently are the use of retarding voltages at the wafer surface (3) and backscattered electron detection (7). While recent results are promising, more progress is needed here.

Electrical Probe Metrology

Comprehensive patterning equipment evaluations can require extremely large numbers of CD measurements in order to accurately capture important effects in photo and etch (9). An example is testing of stepper lens CD uniformity as a function of feature size and pitch, through focus and NA-sigma space. Due to the rapidity of measurement and superb reproducibility, such large amounts of data are often better collected by electrical probing of resistor structures than by low voltage SEM.

Traditionally, electrical metrology has only been useful for characterization of line patterning in conducting films. However, clever application of electrical metrology can yield useful data concerning spaces and holes in dielectrics (10).

Atomic Force Microscopy

Atomic force microscopy (AFM) has begun to diffuse through the IC industry and reports of use for calibration of low V CD SEMs have appeared (11,12). AFM combines exceptional depth and lateral resolution to offer the lithographer an amazing wealth of information about the resist feature's width, wall angles, and thickness. Unfortunately, AFM scan rates are currently very slow, and tip shape and stability have significant impact on measurement accuracy and reproducibility.

AFM probe widths have tracked the SIA Lithography minimum feature size in development; the current state of the art for tip width is about 180 nm, sufficient to image spaces in resist appproximately 180 nm wide. An important question is whether AFM tips can continue to scale with the roadmap, i.e., whether robust tips of 100 nm width and below can be fabricated.

At present, AFM is too slow to be used for real-time imaging or high speed CD measurements. However,development of higher speed scan rates and multiple arrays of independent AFM probes may allow workers to overcome these restrictions in the next several years (13).

Conclusions and challenges

To keep up with the daunting pace of Moore's Law, micropatterning engineers need many improvements in metrology. We primarily need, as Feynman called for, better resolution, and correspondingly better measurement reproducibility, and secondarily, increased data acquisition rates and improved analytical methods.

A problem of key importance in microprocessor production is gate linewidth control. Metrology for this application is not fully adequate to the job. Low voltage SEM, AFM, and electrical probe metrology can all play different and useful roles, but each must be improved.

Memory production requires high resolution SEM and AFM imaging of layers that are now, finally, too small for production to see with the optical microscope.

Here are some general challenges from the author: low voltage SEM resolution should be improved by 5 to 10X over the next ten years. AFM imaging rates (at resolution) should improve by 100-1000X over the same time.

Acknowledgements

I would like to thank the following friends and colleagues for contributing to this talk: Kathryn Wilder and Cal Quate - Stanford University; Bhanwar Singh, Regina Schmidt, Anna Minvielle - AMD, APD Litho; Gary Seligman, Greg Goodwin - AMD, Fab 25; Alan Schwartzman - Brown University; and Ken Morisaki - Fujitsu.

References

1. Richard P. Feynman, "There's plenty of room at the bottom", Engineering and Science, pp22-36, Feb. 1960

2. D.J. Smith, "Achievement of atomic resolution electron microscopy", J.Electron Microscopy Technique, 12:11-23, 1989.

3. M. Ezumi, et al, "Development of critical dimension measurement scanning electron microscope for ULSI (S-8000 series)", SPIE Vol. 2725,105, 1996

4. D.G. Chesebro, et al, " Overview of gate linewidth control in the manufacture of CMOS logic chips", IBM.J.Res.Develop., Vol.39, No.12, pp189-200, Jan/Mar 1995

5. Science, 275, 1069, 2-21-97

6. W.H. Arnold, B. Singh, K. Phan, "Linewidth metrology requirements for submicron lithography", Solid State Technology, pp139-145, April 1989

7. K. Monahan, et al , "Benchmarking multimode CD-SEM metrology to 180nm", SPIE 2725, 1996

8. D. Nyyssonen, "Collection of low energy secondary electrons and imaging in a low voltage SEM", Proc. SPIE, Vol. 2725, pp562-571, 1996

9. C.Yu, A. Minvielle, C. Spanos, "SEM characterization of etch and develop contributions to poly-CD error", SPIE 2725, 169, 1996

10. R.Schmidt, C. Spence, "Process latitude and CD bias evaluation of attenuated PSM", SPIE, 3051-11, 1997

11. H.M. Marchman, "Nanometer-scale dimensional metrology with noncontact atomic force microscopy", SPIE 2725, 527, 1996

12. K. Wilder, B. Singh, W.H. Arnold, "Sub-0.35-micron critical dimension metrology using atomic force microscopy", Proceedings of SPIE, Vol. 2725, 540, 1996

13. S.Manalis, S. Minne, C. Quate, Appl.Phys.Lett.68 (6), 871, 1996