JATIS Journal of Astronomical Telescopes, Instruments, and Systems

RESEARCH PAPER

Development of space-flight room-temperature electronics for the Line Emission Mapper Microcalorimeter Spectrometer

Kazuhiro Sakai,[a,b,*] Joseph S. Adams,[a,b] Simon R. Bandler,[a] Si Chen,[c] Manuel Gonzalez,[c] Damien Prêle,[c] Carl D. Reintsema,[d] Adam J. Schoenwald,[a] Stephen J. Smith,[a] Terrence M. Smith,[a] and Nicholas A. Wakeham[a,b]

[a]NASA/GSFC, Greenbelt, Maryland, United States
[b]University of Maryland Baltimore County, Baltimore, Maryland, United States
[c]AstroParticle and Cosmology Laboratory, Paris, France
[d]National Institute of Standards and Technology, Boulder, Colorado, United States

ABSTRACT. We are developing space-flight room-temperature readout electronics for the Line Emission Mapper (LEM) Microcalorimeter Spectrometer (LMS) of the LEM mission. The LEM mission is an x-ray probe mission designed to study the physics of galaxy formation. The LMS is optimized for low-energy (0.2 to 2 keV) x-ray emission from extremely diffuse gas. The detector is a hybrid transition-edge sensor (TES) microcalorimeter array with a 33′ outer array and a $7' \times 7'$ inner subarray. The outer array consists of 12,736 square pixels on a square grid with a 290 μm pitch but in a close-packed hexagonal shape. The inner subarray consists of 784 TES sensors arranged in a square area in the center of the outer array with the same pixel pitch. The outer array uses a sensor with 2×2 thermal multiplexing known as "Hydra," and the inner array consists of a single absorber per TES. The baselined readout technology for the 3968 TES sensors is time-division multiplexing (TDM), which divides the sensors into 69 columns $\times$ 60 rows. The components of the room temperature readout electronics are the three boxes of the warm front-end electronics (WFEE) and the six boxes of the digital electronics and event processor (DEEP). The WFEE is an interface between the cold electronics and the DEEP, and the DEEP generates signals for the TDM and processes x-ray events. We present the detailed designs of the WFEE and DEEP. We also show the estimated power, mass, and size of the WFEE and DEEP flight electronics. Finally, we describe the performance of the TRL-6 prototypes for the WFEE and DEEP electronics.

Keywords: microcalorimeter; time division multiplexing; readout electronics

Paper 23082SS received Jul. 20, 2023; revised Oct. 2, 2023; accepted Oct. 3, 2023; published Oct. 18, 2023.

1 Introduction

The Line Emission Mapper (LEM) is a mission concept for an x-ray probe designed to study the evolution of galaxies, with a focus on "Unveiling the Drivers of Galaxy Growth" as outlined in the Astro2020 Decadal Survey.[1] The main goal of LEM is to study the x-ray emissions emanating from warm, exceptionally diffuse gas, such as the circumgalactic medium, the intragalactic medium, and the warm-hot intergalactic medium. LEM will be able to distinguish these emissions from the halo emission of our own Milky Way Galaxy. To accomplish this, LEM uses the

*Address all correspondence to Kazuhiro Sakai, Kazuhiro. Sakai@nasa.gov

LEM Microcalorimeter Spectrometer (LMS), a microcalorimeter array with high spectral resolution and sensitivity in the soft x-ray region.[2,3] The LMS, with its large effective area of 1600 cm^2 at 0.5 keV, covers a field of view (FOV) of $30' \times 30'$ with an angular resolution of $10''$. This makes the "grasp" (effective area × FOV) exceptionally large to effectively collect more x-ray photons.

The baselined readout method for the LMS is time division multiplexing (TDM).[4–6] In TDM, the detector sensors are logically organized into a matrix of columns and rows, and multiple rows are read out from a single column (or channel). Multiplexing is achieved using superconducting quantum interference device (SQUID) multiplexers (hereafter SQ1 mux) at the coldest stage.[6] The signal from SQ1 mux is amplified in the SQUID series array (SSA)[7] and connected to the electronics at room temperature. At room temperature, there are boxes called the warm front-end electronics (WFEE) that contain low-noise amplifiers (LNAs) to amplify the signals from the SSA. Signals from the WFEE are then fed to the digital electronics and event processor (DEEP), where the amplified signal is digitized and processed to determine feedback signals for the SQ1 mux and the SSA. The DEEP is also responsible for processing x-ray events and calculating the value of the energy equivalent of the incident x-ray photons for each event.

In this paper, we present a detailed design and provide the current best estimates for the power, size, and mass of the WFEE and DEEP. In Sec. 3, we describe the design and provide resource estimates for the WFEE. In Sec. 4, we describe the design and provide resource estimates for the DEEP. Finally, in Sec. 5, we describe results from a TRL-6 prototype of the DEEP electronics.

2 Time-Division Multiplexed Readout System Overview

The LMS detector is a hybrid array consisting of an outer array and an inner array, as shown in Fig. 1. The number of TESs that can be read out using TDM is limited by the practical considerations of the focal plane assembly (FPA) size (and hence low-temperature cooling power because the heat load scales with the mass of the FPA) and the number of wires in harnesses that are possible considering wiring complexities and heat loads. To cover the area equivalent to a $30' \times 30'$ FOV with relatively small $15''$ pixels, the pixels on the main array are thermally multiplexed using a "Hydra" consisting of four (2×2) absorbers thermally coupled to a single TES sensor with thermal links of differing thermal conductance. The difference in conductance results in different characteristic rise times and pulse shapes for each of the four absorbers. These relatively small variations enable discrimination between the absorbers based on pulse shape.[8,9] There are 3184 such sensors; thus the number of pixels is 12,736 for the outer array. On the other hand, the inner array consists of single absorber TESs covering the inner $7' \times 7'$ FOV, with 784 sensors and the same number of pixels. Both arrays are designed to maximize the

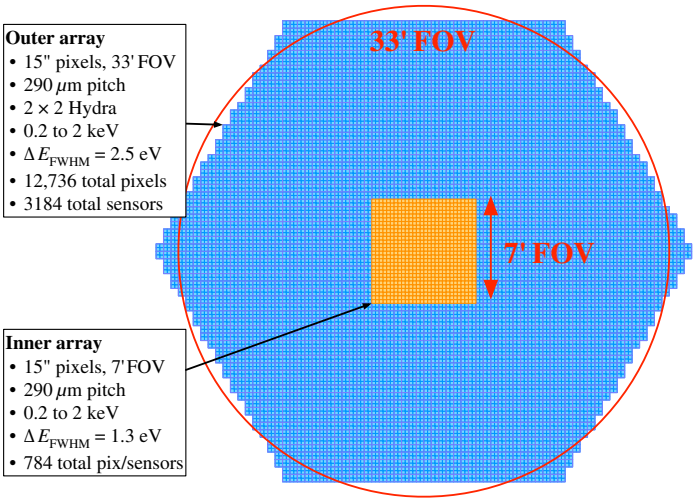

Fig. 1 Baselined focal plan layout of the LMS. It consists of the hexagonal outer array (blue) and the square inner array (orange).

Table 1 Summary of the TES/antico arrays and their readout methods.

	LMS main array	LMS internal subarray	Antico array
Number of sensors	3184	784	12
Number of pixels	12,736	784	12
Hydra	2 × 2	—	—
# of TDM columns	69		3
# of TDM logical rows	60		4
# of TDM physical rows	16 (6 CS + 10 PS)		4
TDM line rate	6.25 MHz		
TDM frame rate (sampling frequency)	104 kHz		1.5 MHz

energy resolution over the energy range of x-rays from the LEM telescope of 0.2 to 2 keV, with an energy resolution of 2.5 eV at 1 keV for the outer array and 1.3 eV at 1 keV for the inner array.

An anti-coincidence (antico) array is located under the TES array to detect high-energy cosmic ray events that deposit some energy in the LMS detector. The detail of the antico is discussed elsewhere in a special JATIS issue.[2,3] Any coincident events on the LMS detector and the antico array are rejected as non-x-ray events in the data processing pipeline that runs on the ground. The antico array also consists of TESs and is read out by the same electronics at room temperature. There is a total of 12 antico sensors. Table 1 gives an overview of the LMS and antico arrays.

For reading out 3968 LMS sensors and 12 antico sensors with TDM, 69 and 3 columns are allocated to each, respectively. For the LMS, 60 sensors are multiplexed as 60 rows per column. These 60 rows are reorganized into another matrix of 6 cluster-select (CS) × 10 pixel-select (PS) using the two-level switch for the multiplexer SQUID.[10] The number of row address lines needed is thus reduced from 60 logical rows to 16. For the antico, a simple SQUID multiplexer is used, and there are four rows. The TDM line rate is baselined to 6.25 MHz, making the frame rate (or sampling frequency) 104 kHz (or 104 ksps) for the LMS and 1.5 MHz (or 1.5 Msps) for the antico. Table 1 also summarizes these TDM parameters for each array.

Figure 2 shows the simplified system diagram of the TDM readout system. For each TDM column, three current DACs in the WFEE provide DC bias currents for the TES, the SQ1 mux,

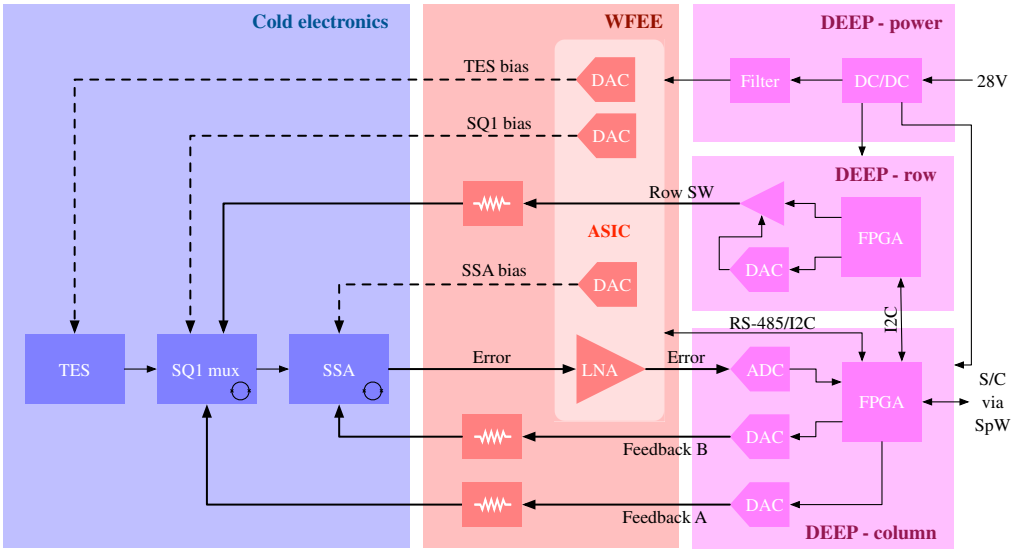

Fig. 2 Simplified system diagram of the TDM readout system. For simplicity, the schematic only shows one TDM column out of 72 total columns. The bold lines are analog fast (~6 MHz) switching signals. The dashed bold lines are DC bias current. All analog signals are differential signals.

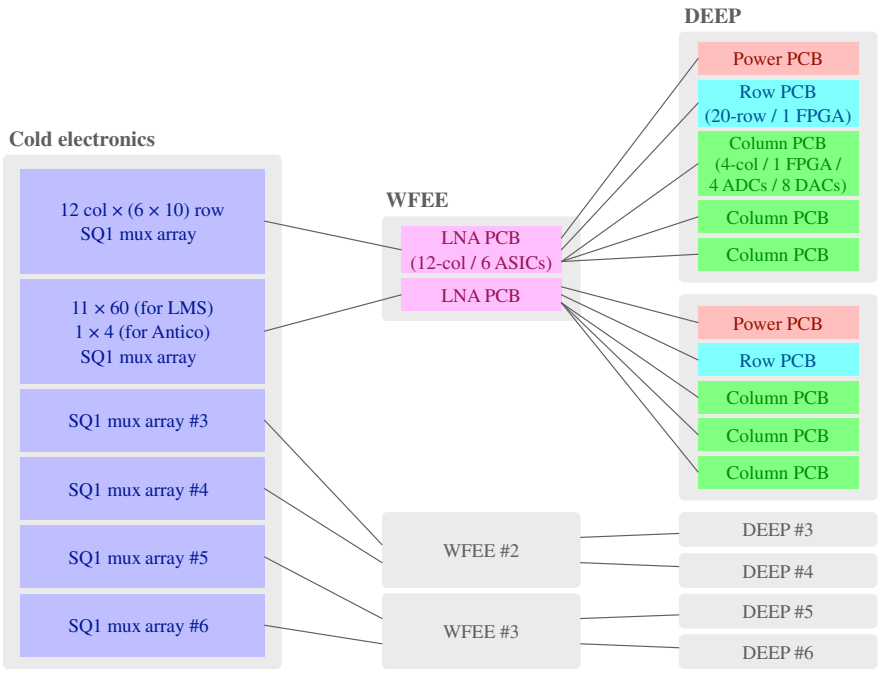

Fig. 3 Segmentation strategy of the readout system. One box of DEEP maps into one WFEE PCB, which reads 12 columns × 60 rows SQ1 mux array (or 11 columns by 60 rows and 1 column × 4 rows SQ1 mux array). Therefore, the system has six segmentations for the LMS and three for the antico.

and the SSA. These DACs reside in a special-purpose application-specific integrated circuit (ASIC), referred to as AwaXe.[11–13] The AwaXe ASIC is currently under development at the Astroparticle and Cosmology Laboratory in Paris and was initially designed for the European Space Agency's Athena X-IFU.[14] Within the ASIC is an LNA to amplify the output signal coming from the SSA. The amplified error signal is interfaced to the column PCB of the DEEP, digitized using a high-speed digitizer ADC, and then processed in an FPGA to generate feedback signals for the SQ1 mux and the SSA at two high-speed DACs. The feedback signals are sent to the WFEE, where passive resistors convert the voltage signals to currents. Another FPGA on the row PCB generates switching signals for the SQ1 mux using high-speed CMOS drivers. The switching signals are connected to the WFEE and converted to currents before being connected to the SQ1 mux. All signals are differential. In the room temperature harnesses, shielded twisted pairs are used to make the connection between the cryostat and the WFEE and between the WFEE and the DEEP. Power for the column and row PCBs is generated on the power PCB, which takes unregulated 28 V from the spacecraft and uses DC/DC converters to generate the required voltages. The WFEE voltage is also generated on the power PCB. These generated voltages are filtered and regulated with linear regulators on each PCB.

There are three WFEE boxes and six DEEP boxes to read out 72 TDM columns. The LEM is a class C science mission, and for fault tolerance, we use a single string and selectively redundant design for the readout electronics. Therefore, the entire readout chain is divided into six groups for the main detector array and three for the antico, as shown in Fig. 3. A critical failure of one component of a DEEP box could cause the loss of a limited section of the detector array with up to 720 sensors (12 columns × 60 rows) for the detector array and/or 4 sensors for the antico.

The mission lifetime of LEM is five years, and the targeted launch date is in 2032. The baselined orbit is the Sun–Earth Lagrange point L1, and the total simulated ionizing dose behind 2.5 mm of aluminum is 23 krad for the five years of the mission lifetime. The parts used in the electronics are NASA level 3 parts.[15] All other hardware requirements for the readout electronics are very similar to those for the Athena X-IFU readout electronics because the cold electronics were designed to match the dynamic signal range at room temperature to that of the X-IFU. This allows us to leverage all of the development of electronics from the X-IFU for the LEM electronics. Table 2 summarizes the key driving requirements for the WFEE and the DEEP.

Table 2 Summary of the key requirements for the WFEE and the DEEP.

Parameter	Requirement
WFEE LNA	
Gain	38 dB
Bandwidth	DC: 20 MHz
Input-referred voltage noise	<1 nV/srHz
$1/f$ noise knee	<1 kHz
DEEP column ADC	
Input range	1 Vpp
Input voltage noise	<60 nV/srHz
$1/f$ noise (at 1 Hz)	<3 uV/srHz
DEEP column DAC	
Output range	2 Vpp
Output voltage noise	<40 nV/srHz
$1/f$ noise (at 1 Hz)	<1 uV/srHz
DEEP event processing	
Absolute timing	2 ms

3 Warm Front-End Electronics

The main component of the WFEE is the ASIC that provides the LNA and the current DAC. One ASIC provides two LNAs and six DACs to read out two columns, and there are two PCBs per box with six ASICs for each board to read 24 columns per box. There are also matched resistor pairs to convert voltage to current for the row signals and the feedback signals, as well as voltage regulators to generate ± 1.65 V from the unregulated ± 2.5 V provided by DEEP. The two PCBs are independent of each other, so the readout system can be divided into six groups.

The AwaXe ASIC family has been developed since 2016 and follows the evolution of the Athena X-IFU TES array readout. The design of the ASICs focuses on optimizing performance in terms of noise, thermal stability, radiation tolerance, and power consumption. SiGe BiCMOS technology is used to meet stringent noise requirements, especially at low frequencies, while maintaining tens of MHz of bandwidth. The first ASICs used AMS 350 nm SiGe technology. Radiation hardness, both in terms of total ionizing dose (TID) up to 100 krad and single event latch-up up to 120 MeV $\cdot$ cm^2/mg, was qualified for these designs. This development ended with the AwaXe_v3 (Fig. 4), which contained two fully differential LNAs and ten slow current DACs for reading out two TDM columns.[16] The AwaXe_v3 is now part of the Athena X-IFU WFEE demonstration model.[13]

Due to the semiconductor industry's trend toward thinner nodes, the ST 130 nm SiGe BiCMOS technology has now been chosen. The AwaXe_v4 ASIC was an initial release in this new technology, designed to test the performance of the WFEE's analog circuits, which consist primarily of two LNAs and two 8-bit DACs. One of the LNAs contains input offset compensation, which is important to compensate the output offset of the SSA and thus increase the total usable dynamic range.[17] The measured gain, noise, and linearity of the ST130 AwaXe_v4 LNAs and DACs perform similarly to the previous AMS foundry. The $1/f$ noise is even better at ST due to using PNP transistors instead of PMOS for the load of the gain stages.

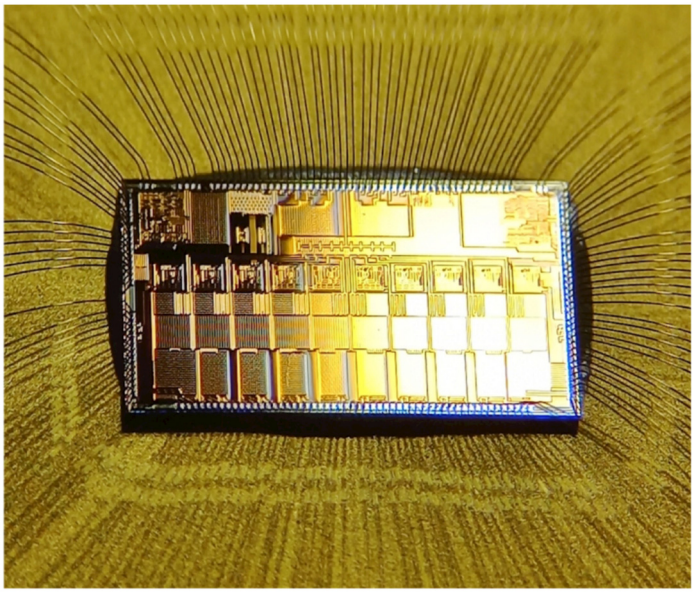

Fig. 4 Photograph of the ASIC "AwaXe_v3." The die size is about 6.75 mm × 3.79 mm, with a pad pitch of 100 μm.

Table 3 Power, mass, and size estimates for the WFEE components.

	Unit power (W)	Unit mass (kg)	Unit size	Qty per box	Power (W)	Mass (kg)
PCB		0.9	10′ × 14′	2	10.9	1.8
ASIC	0.6			12	7.2	
Regulator	0.92			4	3.7	
Frame		0.9	10′ × 14′ × 2′	2		1.8
Cover		0.6	10′ × 14′	3		1.8
Box total					10.9	5.4
System total (3 boxes)					32.7	16.2

Table 3 shows the estimated power, mass, and size of the WFEE. The total power for the three boxes of the WFEE is ∼33 W and ∼43 W with a 30% margin. The total mass is ∼16 kg for three boxes and ∼21 kg with a 30% margin. The size is $10' \times 14' \times 4'$ for each box.

4 Digital Electronics and Event Processing

The DEEP is the core of the readout system. There are six DEEP boxes, as described in Sec. 2, and each DEEP consists of the power PCB, the row PCB, and three column PCBs.

4.1 Row PCB

The row PCB generates the row-switching signals for the SQ1 mux. There are 16 physical rows to switch 60 logical rows. There are also four additional physical rows for the antico. The row PCB consists mainly of a Microchip Technology RTAX2000S FPGA, 10 Renesas ISL7457SRH quad CMOS drivers, and 2 Texas Instruments DAC121S101QML-SP low-speed 12-bit DACs with Analog Devices AD8138S high-speed differential buffers. There is also a Texas Instruments CDCM7005-SP PLL to generate the 125 MHz master clock for the row FPGA and the 3 column PCBs in the same DEEP box. All of these parts are radiation-hard or radiation tolerant.

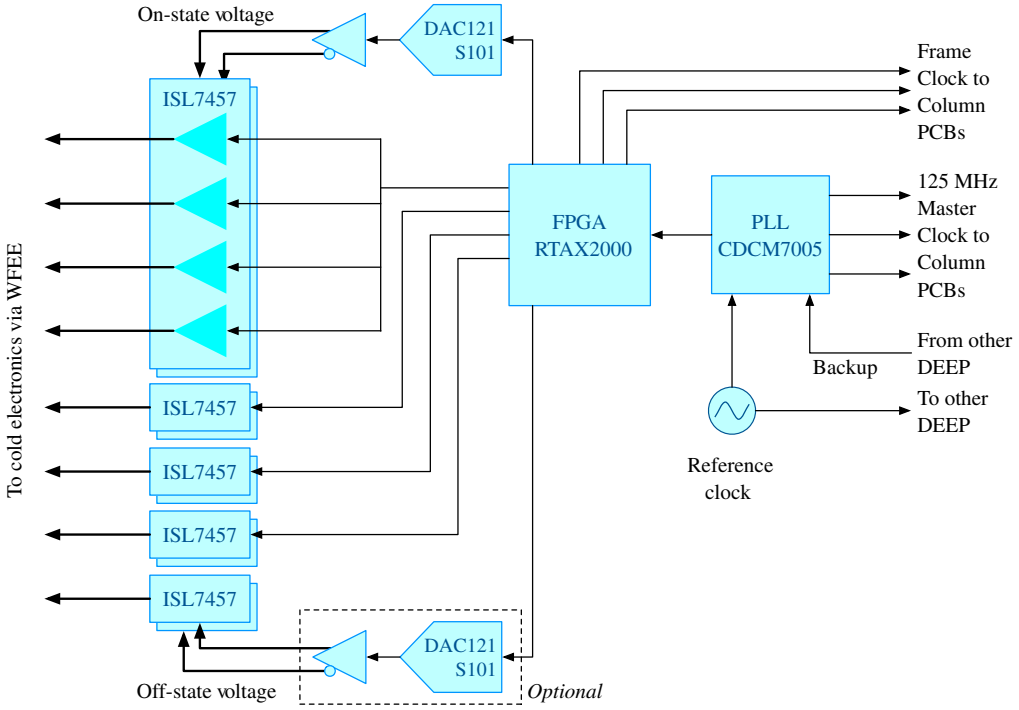

Fig. 5 Simplified schematic diagram of the DEEP row electronics.

Figure 5 shows the schematic diagram of the row PCB. The FPGA generates digital row-switching signals and feeds them into the CMOS drivers. There are two drivers for each row, each in a different chip to generate a differential signal, and the FPGA provides a complementary signal to the second driver for each row. The CMOS drivers provide one of two analog values (on/off) depending on the digital signal. The two DACs generate the value of the two analog signals. The differential drivers on the DAC outputs are used to create the negative voltages fed into the CMOS drivers that generate the complementary side of the signals. The off-state voltage can often be set to 0 V, and achieving the same performance as a non-zero off-state voltage is still possible. Therefore, we consider the DAC and the buffer for the off-state voltage optional and can omit them in the final flight electronics.

The master clock generated by the PLL controls the FPGA and the column PCBs. The frequency is 125 MHz, except that it is scaled down to 1/2 or even 1/4 for the row FPGA. The TDM line rate is 6.25 MHz, 1/20 of the 125 MHz, and the row FPGA's drive frequency can be any multiple of the line rate. For the column PCBs, the master clock is used without downscaling. The row FPGA also generates the TDM frame clock, which is ~104 kHz (= line rate/number of rows), and feeds it into the column PCBs.

One of the six row PCBs will be the source of the reference clock and will distribute it to other DEEP boxes. The distribution will be in a cascaded chain, and the signal delays at each DEEP box will be compensated for in the PLL on the row PCBs. All DEEP boxes can become the source, and in the case of failure, one of the other row PCBs becomes the source. The same is true for the frame clock except that the delays are compensated for in the row FPGAs.

4.2 Column PCB

The main functions of the column PCB are as follows: (a) to demultiplex the TDM signals, (b) to generate feedback signals for SQ1 mux and SSA, (c) to process x-ray events and calculate photon energies, and (d) to communicate with the other components. There are 72 columns in the system, and each column PCB reads out four columns. The column PCB mainly consists of a Xilinx/AMD UltraScale XQRKU060 FPGA, a Texas Instruments CDCLVP111-SP clock buffer, four Analog Devices AD9254S high-speed 14-bit ADCs, and eight Texas Instruments DAC5675A-SP high-speed 14-bit DACs. The differential drivers for the ADCs and DACs are analog devices AD8138S. There is also an external memory (SRAM or DRAM) for the FPGA,

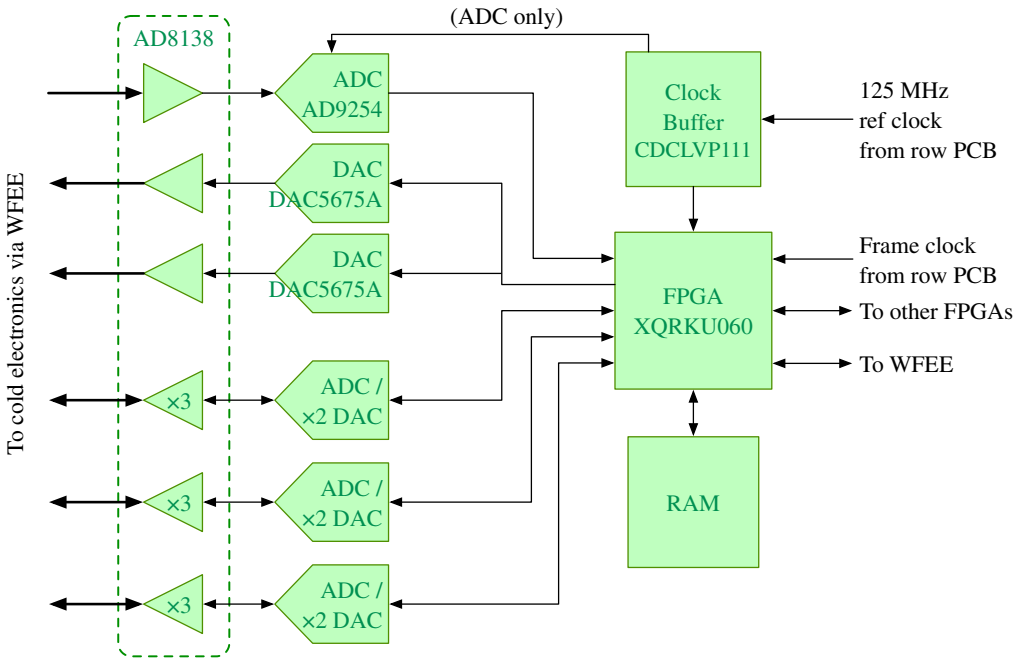

Fig. 6 Simplified schematic diagram of the DEEP column electronics.

but we have not specified a component at this point. All of the above components are radiation-hard or radiation tolerant.

Figure 6 shows the schematic diagram of the column PCB. The clock buffer receives the 125 MHz master clock from the row PCB, splits it, and passes it to 4 ADCs and the FPGA. The FPGA also receives the frame clock from the row PCB. The ADCs are used to digitize the error signal. The FPGA generates two feedback signals using two DACs for each column. The 125 MHz clocks for the DACs are provided by the FPGA.

4.2.1 *Column FPGA design*

Figure 7 shows the block diagram of the FPGA design. The "TDM demux" is the TDM demultiplexer. It is connected to the ADC/DAC, processes the error signal, and generates the feedback signals. The block has the same functionality as the TDM Demux block in our lab-based commercial-off-the-shelf (COTS) electronics.[18] It also demultiplexes the TDM signal and generates raw data streams for each TES pixel.

The raw data stream is sent to the "trigger" block, where the signal is first processed to calculate the derivative and then triggered at a specified threshold. This works like a simple slope

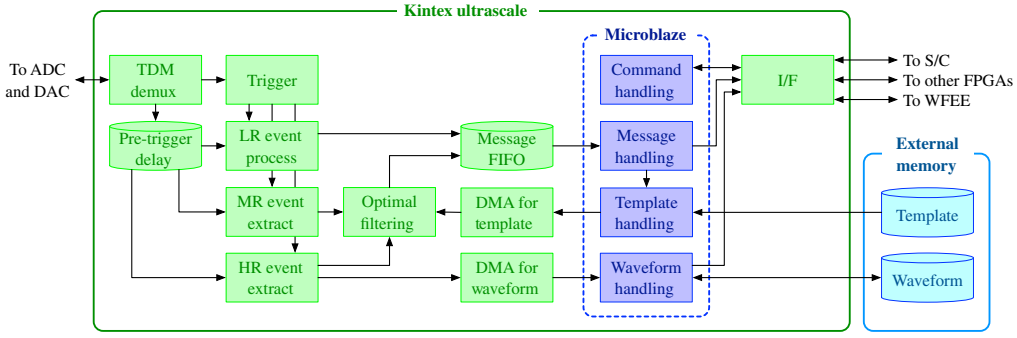

Fig. 7 Block diagram of the DEEP column FPGA design. The green boxes are function blocks that run in the FPGA fabric. The blue boxes are function blocks that run in the MicroBlaze soft-core processor. The cyan boxes are the buffers in the external memory.

Table 4 Thresholds for the intervals to the previous/next trigger, record length, and pretrigger length for each grade.

Grade	HR	MR	LR
Δt_p (ms)	>55	>20	—
Δt_n (= post-trigger length) (ms)	>74	>18	—
Record length	8192 samples/79 ms	2,048 samples/20 ms	24 samples/230 μs
Pretrigger length	512 samples/5 ms	128 samples/1.2 ms	8 samples/77 μs

trigger. For each trigger event, a 16-bit trigger identification number (trigger ID), a 48-bit absolute timestamp, and a 16-bit relative timestamp are assigned and sent to other blocks. The absolute timestamp is a 48-bit integer incremented on each frame clock and reset only on a system-wide reset. The relative timestamp is reset every 10 s based on the pulse-per-second signal from the spacecraft. This relative timestamp is used in the scientific data packets and the absolute timing requirement of 2 ms can be easily met.

Depending on the intervals from the current pulse to the previous pulse (Δt_p) and the next pulse (Δt_n), each event is classified into three event grades: high-resolution (HR), medium-resolution (MR), and low-resolution (LR) grades, as implemented in the Suzaku and Hitomi missions.[19,20] All of these event grades are captured, and the HR event has a full record length of 8192 samples, whereas the MR event and the LR event have shortened record lengths of 2048 and 24, respectively. For HR and MR event grades, optimal filtering is performed to calculate the incident x-ray energy.[21] By contrast, no optimal filtering is performed for LR events, and a raw pulse height is derived, which is simply the height of the pulse. Table 4 summarizes the thresholds, record lengths, and pretrigger lengths for the three event grades.

The raw data stream from the TDM Demux block also goes to the "pre-trigger delay" block. This block generates three data streams with the specified three different delays for LR, MR, and HR and passes these data streams to the "LR event process," "MR event extract," and "HR event extract" blocks.

The LR event process block calculates a raw pulse height and a pulse rise time for each x-ray event once a trigger event is fired at the trigger block. Before the calculations, the data stream is filtered through a boxcar filter with a tap size of 4. The pulse height is the maximum minus the minimum of the data stream after the boxcar filter within the LR event window size of 24. The minimum value of the data stream is also used as the baseline (or offset) of the event. The rise time is the maximum of the differences of the data stream separated by four samples within the same window. The calculated raw pulse height, rise time, and baseline are packed into a message along with the pixel number (a combination of column and row numbers), the trigger ID, and the relative timestamp. The message is then sent to the processor via the "message FIFO" block, a Xilinx/AMD AXI Streaming FIFO.

The MR event extract and HR event extract blocks are the same function blocks. Once a trigger event is fired, they start storing the incoming data stream in one of the 512 sample long chunk buffers, allocating two buffers (double buffers) to each pixel. Before storing the data, they use the absolute timestamp to calculate the interval until the last trigger and store the data only if the interval exceeds the MR and HR grades threshold. It also waits for the next trigger event while storing the data and stops storing data when it occurs. When the chunk buffer is full, it switches to the other buffer to store more data, and the data in the full buffer are flushed to the "optimal filtering" block. These blocks store and flush the data until the total number of extracted samples reaches the length of the MR or HR event records for each x-ray event.

The optimal filtering block receives the chunked data and performs partial optimal filtering. Each chunk of data is associated with the trigger ID, and the block requests a chunk of the template based on the trigger ID. The "template handling" block in the processor receives the trigger ID, searches for the template data in external memory based on the message previously sent by the "LR event process" block, and initiates a DMA transfer for the corresponding chunk of template data. The DMA transfer rate would be the limiting factor for the maximum count rate that

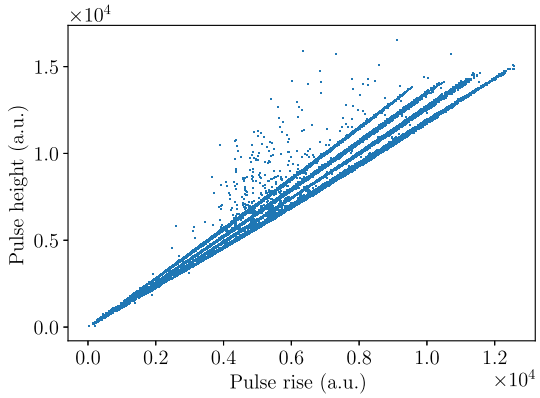

Fig. 8 Example of raw pulse height as a function of pulse rise for an LEM-like 2 × 2 hydra sensor. The details of such hydra designs are shown in Ref. 22.

the system can process. The maximum data transfer rate for the DMA transfer is ∼53 MB/s if the count rate is the theoretical limit (the reciprocal of the HR record length) for all 60 sensors for each of the 4 columns. This is much less than a typical throughput (∼400 MB/s) of the DMA function; therefore, the system should support the theoretical count rate limit. For the Hydra pixels, the template is different for each Hydra pixel, so differentiation of the Hydra pixels must be done before searching for a template. This is done simply by the ratio of the raw pulse height to the pulse rise time. Figure 8 shows an example of a scatter plot of raw pulse height and pulse rise time measured on the LEM-like hydra TES. For each TES sensor, we can define the regions. The raw pulse height and pulse rise time are used to select a suitable template based on these regions.

The optimal filtering is performed nine times for each chunk, shifting the template by −4 to +4 samples. These operations are performed in parallel, and for this purpose, the template sent from external memory has an additional ±4 samples at the beginning and end of the chunk (Fig. 9). Once the partial optimal filtering is completed, the calculated values are packed into a message with the trigger ID and sent to the message FIFO.

The HR event extract can also DMA-transfer the chunked data to the external memory via the "DMA for waveform" block if this is required for diagnostic purposes. The "waveform handling" block reconstructs the entire waveform from the chunked data once all chunks are received. This is used in pulse and noise acquisition to produce an averaged pulse and noise for pixels. It is also used to collect $V - \Phi$ responses for SQ1 and $I - V$ responses for TES. The block sends the waveform data to the spacecraft data recorder on request. In the current baseline, the DEEPs do not generate templates on board. When templates need to be regenerated, we download the average pulses and noise from the spacecraft, generate the templates on the ground, and upload them back to the spacecraft.

The last part of x-ray event grading is done in the "message handling" block in the processor. When an event is an HR event, the block will receive all HR optimal filter messages. Once all HR

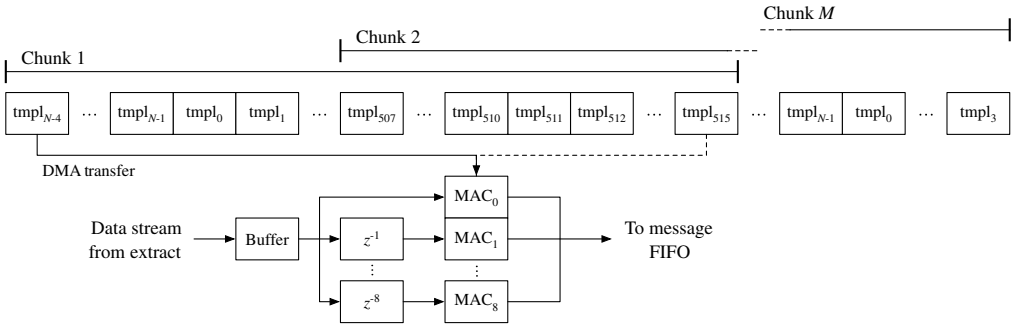

Fig. 9 Parallelization of nine optimal filtering. tmpl_i is the template data, where $N - 1$ is the length of the template. z^{-i} is a discrete-time delay element. MAC is a multiply-accumulate operator.

Table 5 Power and mass estimates for the DEEP components.

	Unit power (W)	Unit mass (kg)	Unit size	Qty per box	Power (W)	Mass (kg)
Row PCB		0.7	8′ × 10′	1	4.1	0.7
FPGA	2.0			1		
DAC	0.05			2		
Driver	0.1			10		
PLL	1.0			1		
Column PCB		0.9	8′ × 10′	3	57.6	2.7
FPGA	10.0			3		
ADC + driver	0.55			12		
DAC + driver	0.75			24		
Clock buffer	1.0			3		
Power PCB				1	28.8	0.9
Digital (70%)	26.4			1		
WFEE (70%)	2.3			1		
Frame		0.9	8′ × 10′ × 1′	5		4.5
Cover		0.35	8′ × 10′	6		2.1
Box total					90.5	10.9
System total (6 boxes)					542.9	65.4

messages are received, it grades the event as an HR event. It also accumulates the partial optimal filter values. For an MR event, the block must have received all MR optimal filtering messages followed by a new LR event message with a new trigger ID. The block can therefore grade it as an MR event once the new LR event is received. The values for partial optimal filtering are also accumulated for the MR event from the multiple messages. Similarly, for an LR event, as soon as the block receives a new LR event with a new trigger ID before it receives the MR optimal filtering message, it can grade it as an LR event.

If a received event is an MR or HR event, the block selects the largest optimal filter value among nine values after collecting all of the messages. The largest value should be within the seven values in the middle. If this is not the case, the event is marked invalid. Using the largest value and two neighboring values, the block calculates the maximum of the second-order fitted polynomial and uses it as the representative optimal filtered value. The block also calculates the phase of the maximum value in 14-bit precision, which refers to -0.5 to $+0.5$, with -0.5, 0, and $+0.5$ corresponding to $(m-1)$, m, and $(m+1)$, respectively, where m is the index of the maximum. This phase corresponds to a subsample timing of the triggered time.

The block packs the trigger time (the relative time), pixel number, raw pulse height, pulse rise time, baseline, MR/HR optimal filter values, and MR/HR phases into a SpaceWire CCSDS packet and sends it to the spacecraft data recorder via the "I/F (interface)" block to complete the grading. If the MR/HR optimal filter values and phases are unavailable due to lower grades, they are simply padded with 0. Any anomaly that occurs during signal processing is marked and noted in the data packet.

For antico events, we treat all events as LR events, so no optimal filtering is applied. Thus the data packet does not have optimal filter values and phases. The detection of events coincident with the main detector events is performed in the data process pipeline on the ground.

Finally, the "command handling" block in the processor processes all commands from the spacecraft. One of the three FPGAs for the column in the box becomes the primary FPGA and

controls the other FPGAs. The primary FPGA interfaces to the WFEE via the I/F block using I^2C and RS-485 to set the DAC currents and read the housekeeping values based on the spacecraft commands.

4.3 Power, Mass, and Size for DEEP

Table 5 shows the estimated power, mass, and size of the DEEP. The unit powers on the power PCB for the digital electronics (row/column PCBs) and the WFEE are the power loss assuming 80% efficiency. The total power for the six boxes of the DEEP is ~543 W and ~706 W with a 30% margin. The total mass is ~65 kg for the six boxes and ~85 kg with a 30% margin. The size is $8' \times 10' \times 5'$ for each box.

5 TRL Maturation Plan

5.1 WFEE

Figure 10(a) shows the noise and gain of one of the AwaXe_v4 LNAs with a 100 Ω load resistor at room temperature to emulate the dynamic impedance of SQUID, connected with a 100 Ω lead pair. The bandwidth is about 30 MHz with input and output matching. The measured input noise is obtained with a 100 Ω source impedance at room temperature. The noise thus includes both the equivalent input voltage and the current noise of the LNA. The white noise in this measurement is dominated by the Johnson noise of the 100 Ω resistor and should be lower than the noise from the SSA for a cryogenic source (~0.5 nV/srHz).[23] The division of the noise by 2 is due to the use of active input matching.[24]

A current source is fundamentally limited by the shot noise of the last transistor stage of the DAC with the minimum fundamental noise of $i_{n_{\min}} = \sqrt{2qI_{\mathrm{DAC}}}$, where q is the elementary charge of an electron and I_{DAC} is the DAC current. At 1 mA, the fundamental limit for a single transistor is about 18 pA/srHz. Here the DAC with mirrors and differential structures is only about two times this fundamental limit and exhibits <40 pA/srHz in white noise. Figure 10(b) shows the measured current noise at the output of the DAC for a current of 500 μA and 1 mA. The noise measurement at 500 μA of about 25 pA/srHz is compatible with the scaling of the noise with $\sqrt{I_{\mathrm{DAC}}}$.

Improved versions of these LNAs and DACs were developed as a minor update to AwaXe_v4 and sent for fabrication in July 2023. This AwaXe_v4.5 fixes LNA instability and has 10-bit wide current sources instead of 8 bit. Linearity and $1/f$ noise have also been improved. In addition to AwaXe_v4.5, a new version, AwaXe_v5, has also been developed; it includes an RS485/I2C communication bus for setting and reading DAC values and controlling the offset compensation of the LNA. A new communication protocol is used for the communication bus, which is built with a rad-hard digital library that includes triple modular redundancy and single-event upset autocorrection. The AwaXe_v5 was also sent for fabrication in the same run as the AwaXe_v4.5.

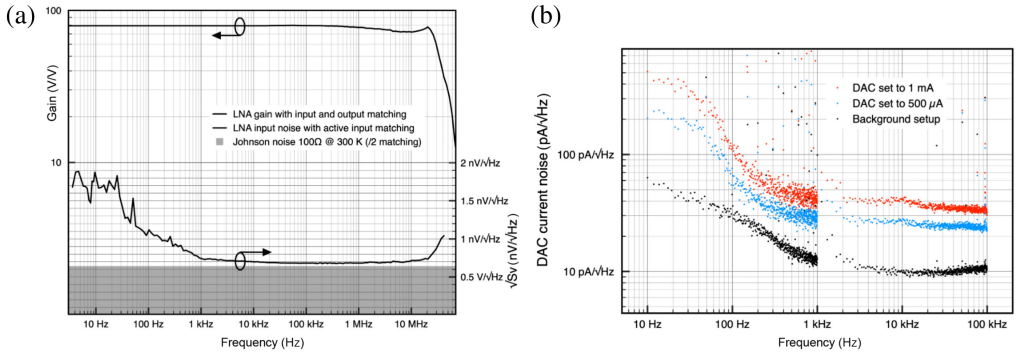

Fig. 10 (a) Measured noise and gain of the AwaXe_v4 LNA with a 100 Ω load resistor. (b) Measured noise of the current DAC for a current of 500 μA and 1 mA.

TID tests will be conducted with the AwaXe_v4 to validate the ST technology in October 2023. Single-event effects will also be tested after the AwaXe_v5 is delivered in early 2024. The ASIC, and therefore the WFEE, will be TRL-6 after these radiation tests.

5.2 DEEP

We have already developed the TRL-6 prototype for the DEEP. It is based on COTS electronics that we developed for laboratory purposes.[18] The COTS electronics uses the Xilinx/AMD KCU105 FPGA evaluation board for the column electronics, which is equipped with an FPGA of the same family (UltraScale Kintex) as the LEM flight electronics, so it is considered a prototype board for the flight FPGA.

To use the same FPGA board as the COTS electronics, we developed an ADC/DAC daughter card with a low pin count FPGA mezzanine card (FMC) connector (Fig. 11). The card contains an AD9254 ADC and two DAC5675A DACs, the commercial equivalent of flight ADC and DAC, to read out one TDM column. The AD8138, a commercial version of the flight differential driver, is used for the ADC and DAC front ends. At the input and output of the ADC and the DAC are 50 MHz seventh-order Bessel low-pass filters for anti-aliasing. In addition, a Texas Instruments LMH6628 is used as a high-impedance receiver at the ADC input; it can be omitted in the flight electronics, which will have an input impedance of 100 Ω in the current baseline. The card also has a CDCLVP111, the commercial equivalent of the clock buffer for flight. Because of the available I/O pins, only 12 MSB bits are wired to the second DAC. The FPGA board generally provides three voltages, +12 V, +3.3 V, and VADJ (+1.8 to +3.3 V) at the FMC connector. We used the +12 V to generate +5 V using a buck converter, and from this +5 V, +3.3 V is generated using a low dropout (LDO) regulator. From the +5 V, a low-noise DC/DC converter is also used to generate ±6.5 V, which is finally converted to ±5 V using LDO regulators. Finally, +1.8 V is generated from the +3.3 V provided by the FPGA board using an LDO regulator. These voltage converters and regulators are specifically needed to generate the required voltages from the voltages provided by the FPGA board, and they are different from the converter/regulators that will be used in flight electronics. Therefore, these parts are not suitable for flight. We also used a non-flight voltage reference, the LTC6655 from analog devices, for the initial testing of ADC and DAC. We plan to replace this with the REF43 from analog devices, in which there is a flight-qualified version, the REF43S.

We redesigned the row electronics of the COTS electronics to replace the components with the part that we chose for the flight electronics, as shown in Fig. 12(a). The board is equipped with 20 EL7457, commercially equivalent to the flight part ISL7457, to have 40 differential row outputs. The output voltages are set by two DAC121S101 followed by AD8138, which are also commercially equivalent to the flight DAC and differential driver. The PLL components in the original electronics were also replaced with a commercial version of the CDCM7005. Although the flight FPGA for the Row PCB is the RTAX2000, due to the availability of the RTAX prototypes, we used the same AVNET MicroZed board equipped with the Xilinx/AMD Zynq-7000 SoC as the original COTS electronics.

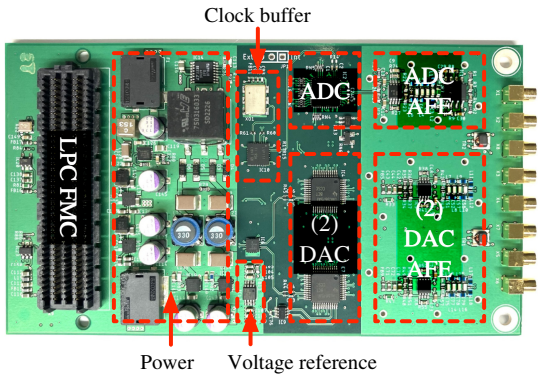

Fig. 11 Developed ADC/DAC daughter card to use with the COTS electronics FPGA board.

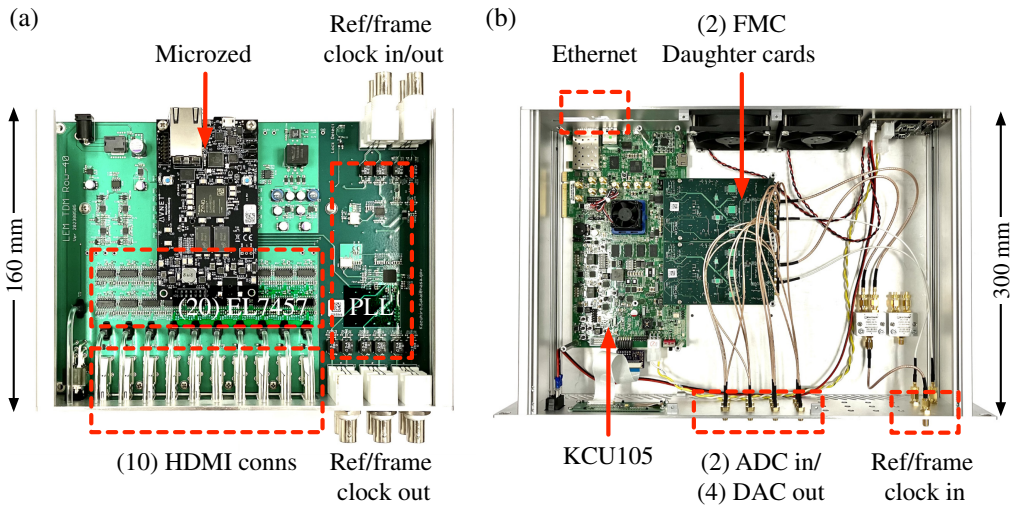

Fig. 12 TRL-6 prototype on (a) the row electronics and (b) the column electronics.

We connected two of the developed daughter cards to a KCU105 board for the column electronics, as shown in Fig. 12(b). The same firmware was used as the COTS electronics, but the system was clocked at 125 MHz supplied by the row prototype. The firmware performs triggering and recording x-ray events in the FPGA but does not process these events on board. Instead, it sends the triggered records to a host computer via the Ethernet, and all event processing and data analysis occur after all events are recorded.

Figure 13(a) shows the measured noise for the ADC and the DAC on the column electronics. The white noise levels for the ADC and DAC are 19.5 and 17.6 nV/srHz, respectively, whereas the $1/f$ noise levels at 1 Hz are 2.42 uV/srHz and 633 nV/srHz. These noise levels are measured at input/output dynamic ranges of 1 Vpp for ADC and 2 Vpp for DAC. The roll-off seen at the high-frequency end for the DAC noise is due to the Bessel filter. The measured noise meets the LMS requirements.

Figure 13(b) shows the co-added Mn-Kα energy histogram acquired with the developed DEEP prototype with 2-columns $\times$ 32-rows multiplexing on an Athena test platform.[25] We collected $>20,000$ pulses for each of every 60 pixels with an average count rate of $\sim$0.2 cps/pixel. For optimal offline filtering, we used the same algorithm as for event processing firmware. We measured a ΔEFWHM of 2.01 ± 0.01 eV for the 60-pixel co-added Mn-Kα spectrum, which is consistent with the results that we measured with legacy laboratory NIST electronics and the COTS electronics.[18,25,26]

The voltage reference used in the measurements is still a part that does not exist in the flight version. We will verify the performance after replacing the current voltage reference with REF43, which is available in the flight version.

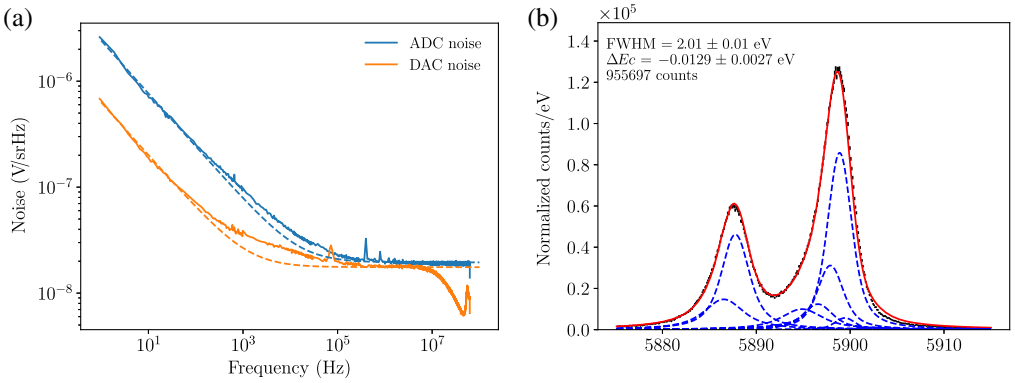

Fig. 13 (a) Measured ADC/DAC noise on the column electronics and (b) 60-pixel co-added 6 keV MnKa spectrum measured in 2×32 TDM.

6 Summary

We designed the space-flight room temperature electronics to read 72 columns in the TDM for the LMS. The WFEE is the analog front end and consists of three boxes with two independent PCBs for each box. The DEEP is the digital electronics, and there are six boxes. The entire readout system is thus segmented into six groups. The estimated power for the WFEE and DEEP is 33 and 543 W, respectively. The estimated mass is 16 and 65 kg, and the size of each box is $10' \times 14' \times 4'$ and $8' \times 10' \times 5'$ for WFEE and DEEP, respectively. The TRL-6 prototype for WFEE was developed and showed an expected performance; radiation testing is planned in early 2024 before TRL-6 is achieved. The TRL-6 prototype for DEEP was also developed and demonstrated expected performance. The prototype performed the 2×32 TDM demonstration for 6 keV x-rays on the Athena test platform and achieved 2 eV FWHM for the 60-pixel co-added spectrum.

Code, Data, and Materials Availability

Data are available from the authors upon request.

Acknowledgments

The material is based upon work supported by NASA (Award No. 80GSFC21M0002).

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Kazuhiro Sakai is an assistant research scientist at the University of Maryland Baltimore County working at NASA Goddard Space Flight Center (GSFC). He received his PhD in physics from the University of Tokyo in 2015. He was a postdoctoral researcher at the Institute of Space and Astronautical Science/Japan Aerospace Exploration Agency from 2015 until he became a postdoc at NASA GSFC in 2016.

Simon R. Bandler is a research astrophysicist at NASA's Goddard Space Flight Center. He received his BS degree in mathematical physics from the University of Sussex, United Kingdom, and his MS degree and PhD in physics from Brown University in 1992 and 1996, respectively. He is the author of more than 200 journal papers. His current research interests include transition-edge sensor and magnetic x-ray microcalorimeters, x-ray astrophysics, and the ESA flagship mission Athena.

Si Chen is a research engineer at the Astroparticle and Cosmology Laboratory (APC). He obtained his PhD in microelectronic instrumentation from the University of Paris in 2019. He specializes in low-noise analogue circuits and full-custom radiation-hardened digital circuits based on SiGe BiCMOS technologies. Since 2016, he has been working on the development of mixed ASICs dedicated to an electronic subsystem, the WFEE, which is the warm front-end stage in the reading chain of the X-IFU instrument in the context of the x-ray space mission Athena.

Manuel Gonzalez is a postdoc at the APC working on the design and characterization of low-noise electronics for cryogenic detectors readout. He joined APC in 2020 after obtaining his PhD in physics from Balseiro Institute, Argentina. There, he worked on the microfabrication of III-V semiconductor heterostructures. He has experience in the design and deployment of scientific instruments, notably for the Pierre Auger Observatory and the QUBIC CMB experiment.

Damien Prêle received his PhD from the Université Pierre et Marie Curie in Paris in 2007. He joined the APC immediately thereafter continuing his work in the field of cryogenic low-noise instrumentation. As a co-investigator for X-IFU Athena and a project manager for the X-IFU warm front-end electronics (WFEE) since 2014, he develops low-noise and low-gain drift ASICs for front-end electronics.

Stephen J. Smith received his MPhys degree in physics with space science and technology and his PhD in physics from the University of Leicester, United Kingdom, in 2002 and 2006, respectively. He is a research astrophysicist working at NASA's Goddard Space Flight Center. He is an author of more than 100 published papers. His primary research interests are in the development of cryogenic detectors for x-ray astronomy applications.

Nicholas A. Wakeham is an assistant research scientist at the University of Maryland Baltimore County working at GSFC. He received his PhD in low-temperature condensed matter physics from the University of Bristol in 2013. He was a postdoctoral researcher at Los Alamos National Laboratory from 2013 until he became a NASA postdoctoral fellow at GSFC in 2016. His interests are exotic electronic states, unconventional superconductivity, and superconducting detectors.

Biographies of the other authors are not available.