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Alternative Lithographic Technologies

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The SPIE Advanced Lithography Symposium is the most important and widely attended symposium on lithography today, typically attracting over 2000 attendees from more than 30 countries. For anyone working in the field and looking to understand the most current trends, the event constantly attracts the most groundbreaking work in the field and attracts the attention of the industry's key decision makers.

The symposium consists of seven individual conferences that are run more or less in parallel. These conferences cover:

- Extreme Ultraviolet (EUV) Lithography
- Alternative Lithographic Technologies
- Metrology, Inspection, and Process Control for Microlithography
- Advances in Patterning Materials and Processes
- Optical Microlithography
- Design-Process-Technology Co-optimization for Manufacturability
- Advanced Etch Technology for Nanopatterning

The Alternative Lithographic Technologies conference showcases novel lithographic and patterning techniques that provide emerging patterning solutions for applications that are scaled (i.e. 16 nm technology integrated circuitry as defined by the International Technology Roadmap for Semiconductors or *ITRS*), scaling-independent, or non-IC related. Our willingness to showcase non-IC related topics makes this conference somewhat unique relative to the other advanced lithography conferences, and opens the door to applications including bioelectronics and genomics, photovoltaics and related energy applications, disk drives and patterned media, flat panel displays, optoelectronics and LEDs, photonic crystals, negative-refractive-index/meta materials and nanopatterned sensors. In particular we welcome contributions on hybrid approaches that employ a combination of two or more lithographic techniques.

Some of the key topics discussed in the conference are directed self-assembly (DSA), alternative pattern integration techniques (including spacer multiple patterning and self-aligned strategies), nanoimprint lithography, maskless lithography, and other novel lithographic approaches.

In this *JM3* special section, we are highlighting seven papers that were presented at the 2014 conference and a review paper on the subject of design rule restrictions. Design rule restrictions is an important and timely subject, as resolution limits have caused many integrated circuit manufacturers to apply self-aligned double, triple, or quadruple patterning processes, which in addition to adding cost to the overall process flow also create patterns that are essentially one-dimensional. In the work presented by Vaidyanathan et al., the authors consider the ramifications of restricting all levels of a 14-nm process flow. They conclude that adopting such an approach leads to inefficient design efficiency and process integration concerns. The authors describe the importance of using design technology co-optimization which includes system-on-a-chip design elements.

There are four papers on directed self-assembly (DSA), a block copolymer pattern densification method that has attracted huge interest in the industry over the last five years. DSA work has focused primarily on two topics: 1) line densification as an alternative approach to the process intensive self-aligned triple and quadruple patterning methods currently being applied in advanced devices such as NAND Flash memory, and 2) contact hole shrinking methods designed to overcome the resolution limits of immersion scanners.

Having good models help drive block copolymer (BCP) research, and Lawson et al. from the Georgia Institute of Technology, report on a simulation of BCP behavior based on molecular dynamics of coarse-grained polymer chains. This model was specifically used to study the effect on the order-disorder transitions. A paper by Yoshimoto et al. takes on the subject of contact hole shrinkage, and applies a simplified Ohta-Kawasaki model to identify the best conditions for minimizing morphological defects in a PS-b-PMMA diblock copolymer system. Bennett et al., describe the inherent limitations of PS-b-PMMA, and discuss whether the blending of liquid ionic additives help to improve both morphology and domain size in these systems. Finally in an example of a non-IC application, Dr. XiaoMin Yang from Seagate

Technology LLC reports on the development of 1.5 TB/in^2 DSA-based process (meaning a half pitch of approximately 11 nm) necessary to fabricate both the memory elements and servo patterns for a patterned media disk drive.

Nanoimprint lithography provides a means of potentially avoiding the design rule restrictions discussed above and has been used to fabricate an extensive variety of devices. As a 1× patterning process, however, a large burden is placed on the fabrication of the mask. Two imprint papers appear in this edition. Helmut Schift, from the Paul Scherrer Institut Laboratory for Micro and Nanotechnology, reviews the process chains necessary to fabricate devices and specifically examines an injection molding approach to form microcantilevers. In the second imprint publication, Ogawa et al. apply a branched and functionalized siloxane, epoxy–Si-12, as a means for reversing the tone of both isolated and dense features patterned using step and flash imprint lithography. The approach is potentially useful for tone reversing patterns formed by many other lithographic technologies as well.

Finally, there is a single paper on the topic of direct write electron beam (e-beam) lithography. Maskless Beam Direct Write (MBDW) has long been studied as an alternative to mask-based approaches such as 193 immersion lithography. Elimination of a mask is particularly cost compelling for short run devices, and presents a potentially fast way of device prototyping. Maskless electron tooling typically utilizes a large number of beams, created either from a single source or through the application of micro e-beam columns, to address the issue of throughput. In this paper, Pieter Brandt, from MAPPER Technology, discusses the methods required to control features exposed with a 5 kV e-beam source. Adjustments to actual feature size, dose modulation and background dose, and combinations thereof, are all considered.

We would like to thank all of the authors for their contributions. We also hope you find these articles interesting and continue to follow the development of alternative lithographic technologies at the conference, in the conference proceedings, and in future special sections in *JM3*.

Douglas J. Resnick is the vice president of marketing and business development for Canon Nanotechnologies. Prior to this role, Doug served as the VP of mask technology and later as the VP of strategic development for molecular imprints. Previously, Doug worked for Motorola Research Labs (1990–2004), where he was responsible for developing the imprint lithography research program. Doug started his career with AT&T Labs (1981–1990), where his development programs included x-ray lithography, e-beam direct write, and plasma etching of photomasks. He has authored or coauthored over 170 technical publications and is an inventor of more than 30 U.S. patents. He has served as the conference chair for both the EIPBN and SPIE Microlithography Symposiums. Doug received his PhD from the Ohio State University in the field of solid state physics.

Christopher Bencher is a distinguished member of the technical staff working in the CTO Office of Applied Materials on Pathfinding and Commercialization of Advanced Patterning Techniques. In 20 years at Applied Materials, Chris has directed research and development in anti-reflective coatings, carbon hardmasks, double patterning integration, and directed self-assembly. Chris has been a leading advocate for the capabilities of sidewall spacer double patterning, publishing annually and working with designers and EDA companies to further extend the SADP patterning technique for logic. Outside of work, he participates on the ITRS lithography roadmap team and co-chairs the SPIE Alternative Lithography Conference.

Ricardo Ruiz manages the Nanofabrication and Self Assembly Group at HGST, a Western Digital Company since 2012, where he oversees nanofabrication strategies for sub-15 nm lithography. His research focuses on directed self-assembly and fundamentals of pattern formation. He joined Hitachi Global Storage Technologies in 2006 as a research staff member, where he introduced directed self-assembly with density multiplication for bit-patterned media applications. Ever since, he has been a strong proponent of self-assembling solutions for patterning applications beyond optical lithography. Prior to these roles, he was a postdoctoral fellow at IBM T. J. Watson and before that at Cornell University. He received his PhD in physics from Vanderbilt University in 2003.